INTEGRATED CIRCUITS

CMOS ICs for Clocks, Watches and Real Time Clocks

Data Handbook IC16
1998



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QUALITY ASSURED

Our quality system focuses on the continuing high quality of our components and the best possible service for our customers. We have a three-sided quality strategy: we apply a system of total quality control and assurance; we operate customer-oriented dynamic improvement programmes; and we promote a partnering relationship with our customers and suppliers.

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All used or obsolete components should be disposed of according to the regulations applying at the disposal location. Depending on the location, electronic components are considered to be 'chemical', 'special' or sometimes 'industrial' waste. Disposal as domestic waste is usually not permitted.

CMOS Integrated Circuits for Clocks, Watches and Real Time Clocks

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Short-form specification	The data in this specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

PURCHASE OF PHILIPS I²C COMPONENTS



Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

Dear Customer,

Philips Semiconductors is one of the most important producers of CMOS integrated circuits for clocks and watches in the world. Situated in Switzerland, the heart of the European clock and watch industry, Philips Semiconductors benefits to a large degree from this unique industrial environment. It is therefore not surprising, that Philips was one of the first semiconductor companies to apply the silicon gate CMOS (complementary metal oxide semiconductor) technology in the production of clock and watch circuits and was the first company to offer an SO package (mini-pack) back in the seventies.

Philips Semiconductors maintains its position at the forefront of the clock and watch IC industry, being the first company to offer the EEPROMs (electrically erasable programmable read only memories), with operating voltages as low as 1.1 v, for time adjustment. This latest development enables the industry to find better technical and cost effective solutions for their products.

To enable the clock and watch industry to maintain its word-renowned quality image, Philps Semiconductors has implemented a Company-Wide Total Quality Management (TQM) program. This TQM program, involving every employee, features a continuous improvement of customer service and product quality. This commitment to quality has lead to us being able to set our standard at zero defect and now enables us to offer our customers a zero defects warranty. The warranty means that if he finds a single device which does not conform to the published specification, the customer can return the complete lot for rescreening or replacement. Faselec is the first company in the world to offer the clock and watch industry a zero defects warranty.

At PhilipsSemiconductors quality dominates all phases of manufacture. Quality is built into the product by the conscious use of advanced technological aids and a continuous monitoring off process steps (SPC) through in-line quality controls. Additionally a stringent incoming inspection of all materials used assures an end-product with an inherently high quality level.

All products are 100% tested against published specifications, any device not conforming to the specifications is rejected. Conformity of each lot to the published specifications is double-checked by our Quality department, which is independent from production.

The dedication of the high-qualified personnel and the large amount of know-how accumulated over the years, backed by constant efforts in developing new process and packaging technology as well as new products, makes Philips Semiconductors the preferred source for your clock and watch circuits.

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ANALOG WATCH CIRCUITS: 32 KHZ

Table 1 Watch circuits overview: PCA146x series

TYPE # PCA....	DELIVERY FORMAT(1)	PERIOD t_T (s)	SPECIFICATIONS						
			PULSE WIDTH t_p (ms)	DRIVE (%)	DETECT CRITERION	EEPROM	BATTERY EOL DETECTION	REMARKS	PAGE
1461	U; U10	1	7.8	max.100 81	P = 1 N = 2	yes	yes	1.5 V and 2.1 V Lithium	28
1462	U; U/7; U/10	1	5.8	max.100 81	P = 1 N = 2	yes	yes	1.5 V and 2.1 V Lithium	
1463	U; U/10	1	3.9	max.100 81	P = 1 N = 2	yes	yes	1.5 V and 2.1 V Lithium	
1465	U/10; U/7	1	5.8	max.100	P = 1 N = 2	yes	no	1.5 V	
1467 .	U/10	1	7.8	max.100	P = 1 N = 2	yes	no	1.5 V	

Note

1. U = chip in tray; U/7 = chip with bumps on tape; U/10 = chip on foil.

Table 2 Watch circuits overview: PCA148x series

TYPE # PCA...	DELIVERY FORMAT(1)	PERIOD t_T (s)	SPECIFICATIONS						
			PULSE WIDTH t_P (ms)	DRIVE (%)	DETECT CRITERION	EEPROM	BATTERY EOL DETECTION	REMARKS	PAGE
1485	U/7	1	5.8	75	P = 1 N = 2	yes	yes		45
1486	U/7	1	5.8	75	P = 1 N = 2	yes	no		
1487	U/5	1	7.8	75	P = 2 N = 3	yes	yes		

Note

1. U = Chip in trays; U/5 = wafer; U/7 = chip with bumps on tape.

Table 3 Watch circuits overview: PCA16xx series

TYPE # PCA...	DELIVERY FORMAT[1]	PERIOD t_T (s)	SPECIFICATIONS					
			PULSE WIDTH t_P (ms)	DRIVE (%)	EEPROM	BATTERY EOL DETECTION	REMARKS	PAGE
1601	U/10	1	7.8	100	yes	no		60
1602	T	1	7.8	75	yes	no		
1603	U/7	20	7.8	100	yes	no		
1604	U/10	5	7.8	75	yes	no		
1605	U/7	5	4.8	75	yes	no		
1606	U/10	10	6.8	100	yes	no		
1607	U	5	5.8	100 75	yes	no	1.5 V and 2.1 V Lithium	
1608	U	5	7.8	100 75	yes	no	1.5 V and 2.1 V Lithium	
1611	U	1	6.8	75	yes	no		
1621	U/7	20	4.8	100	yes	no		
1622	U	1	4.8	100	yes	yes		
1623	U	20	4.8	75	yes	no		
1624	U	12	3.9	75 56	yes	no	1.5 V and 2.1 V Lithium	
1625	U/7	5	5.8	75	yes	no		
1626	U	20	5.8	100	yes	no		
1627	U/7	20	5.8	100 75	yes	no	1.5 V and 2.1 V Lithium	
1628	U	20	5.8	75	yes	no		
1629	U/7	5	6.8	75	yes	no		

Note

1. U = Chip in trays; U/7 = chip with bumps on tape; U/10 = chip on foil; T = SOT144-1.

Table 4 Watch circuits overview: PCA167x series

TYPE # PCA...	DELIVERY FORMAT[1]	PERIOD t_T (s)	SPECIFICATIONS					
			PULSE WIDTH t_P (ms)	DRIVE (%)	EEPROM	BATTERY EOL DETECTION	REMARKS	PAGE
1672	U	1	7.8	56	no	no	3 V Lithium	69
1673	U	1	5.8	56	no	no	3 V Lithium	
1675	U	1/16	5.8	100	no	no	no oscillator	
1676	U/10	10	5.8	56	no	no	3 V Lithium	
1677	U	10	7.8	100	no	no	1.5 V	

Note

1. U = Chip in trays; U/10 = chip on foil.

DIGITAL CAR CLOCK CIRCUITS: 4.19 MHZ QUARTZ CRYSTAL

Table 5 PCF1171C to PCF1179C overview.

TYPE NUMBER	DIGITS	FUNCTIONS[1]									TYPICAL SUPPLY CURRENT (μA)	REMARKS	PAGE
		A	B	C	D	E	F	G	H	I			
PCF1171C	4	•	•		•	•	•		•		400		75
PCF1172C	3½	•		•	•	•	•		•		400		83
PCF1174C	4	•	•	•	•	•	•		•	•	950	note 2	91
PCF1175C	4	•	•	•	•	•		•	•	•	950	note 2	103
PCF1178C	4	•	•	•	•	•		•	•	•	950	note 2	115
PCF1179C	4	•	•	•	•	•		•	•	•	950	note 2, 3	127

Notes

1. Where columns A to I are the functions for:
   - A = 12-hour mode
   - B = 24-hour mode
   - C = AM/PM annunciator
   - D = hours
   - E = minutes
   - F = direct drive
   - G = duplex drive
   - H = internal voltage regulator
   - I = EEPROM.
2. EEPROM for time calibration and voltage regulation of LCD.
3. Set mode with four advances per second.

REAL TIME CLOCK CIRCUITS (RTC)

Table 6 PCF8563 to PCF8593 overview

TYPE NUMBER	I²C-BUS	CLOCK OPERATING SUPPLY VOLTAGE (V)	PACKAGE	REMARKS	PAGE
PCF8563	yes	1.0 to 5.5	DIP8, SO8	• Provides year, month, day, weekday, hours, minutes and seconds • Century flag • Alarm and timer functions	139
PCF8573	yes	1.1 to 6.0	DIP16, SO16	• Provides month, day, hours and minutes • On-chip power failure detector • Alarm register for presetting a time or remote switching function	157
PCF8583	yes	1.0 to 6.0	DIP8, SO8	• Provides month, day, weekday, hours, minutes, seconds and hundredths of seconds • 240 × 8-bit low-voltage RAM • Universal timer with alarm and overflow indication • Automatic word address incrementing	174
PCF8593	yes	1.0 to 6.0	DIP8, SO8	• Provides month, day, weekday, hours, minutes, seconds and hundredths of seconds • 8-byte scratchpad RAM (when alarm not used) • Universal timer with alarm and overflow indication • Automatic word address incrementing	195

Internet World Wide Web Home Page

WHAT IS IT?

Welcome to our place in cyberspace.

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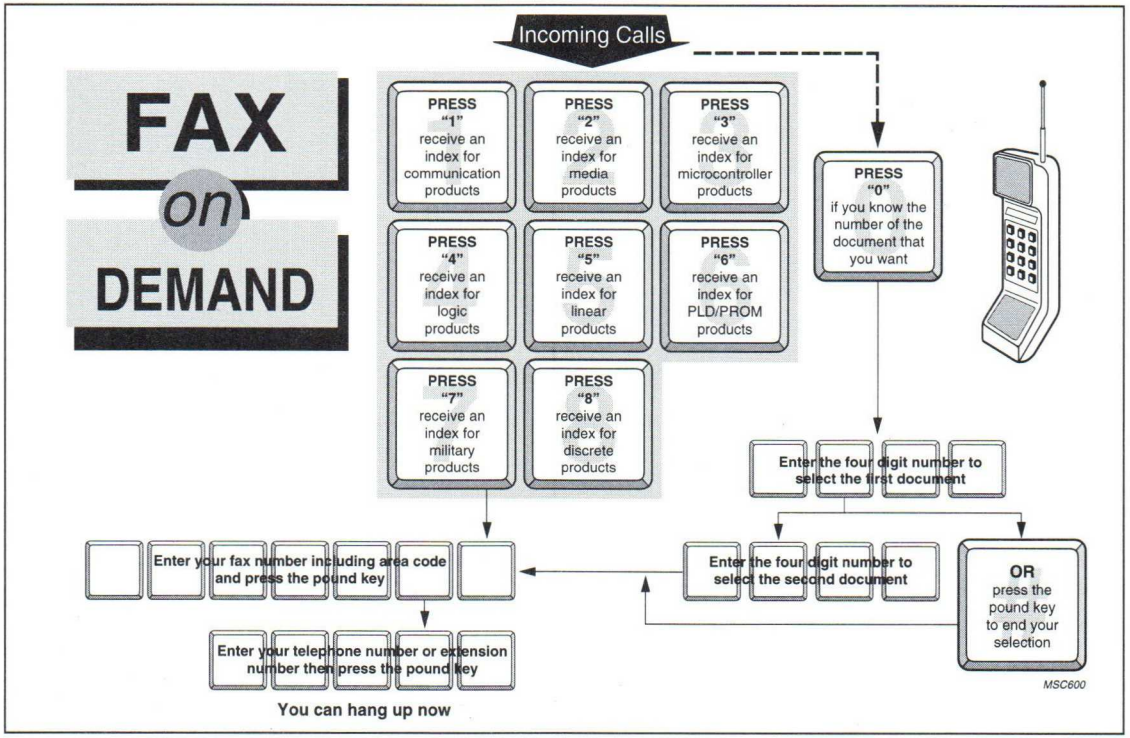
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The FAX-on-DEMAND system is a computer facsimile system that allows customers to receive selected documents by fax automatically.

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To order a document, you simply enter the document number. This number can be obtained by asking for an index of available documents to be faxed to you the first time you call the system.

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Italy	39-167-295502
North America	1-800-282-2000

LOCATIONS SOON TO BE IN OPERATION

- Hong Kong
- Japan
- The Netherlands.

GENERAL

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TOTAL QUALITY MANAGEMENT

Philips Semiconductors is a Quality Company, renowned for the high quality of our products and service. We keep alive this tradition by constantly aiming towards one ultimate standard, that of zero defects. This aim is guided by our Total Quality Management (TQM) system, the basis of which is described in the following paragraphs.

Quality assurance

Based on ISO 9000 standards, customer standards such as Ford TQE and IBM MDQ. Our factories are certified to ISO 9000 by external inspectorates.

Partnerships with customers

PPM co-operations, design-in agreements, ship-to-stock, just-in-time and self-qualification programmes, and application support.

Partnerships with suppliers

Ship-to-stock, statistical process control and ISO 9000 audits.

Quality improvement programme

Continuous process and system improvement, design improvement, complete use of statistical process control, realization of our final objective of zero defects, and logistics improvement by ship-to-stock and just-in-time agreements.

ADVANCED QUALITY PLANNING

During the design and development of new products and processes, quality is built-in by advanced quality planning. Through failure-mode-and-effect analysis the critical parameters are detected and measures taken to ensure good performance on these parameters. The capability of process steps is also planned in this phase.

PRODUCT CONFORMANCE

The assurance of product conformance is an integral part of our quality assurance (QA) practice. This is achieved by:

- Incoming material management through partnerships with suppliers.
- In-line quality assurance to monitor process reproducibility during manufacture and initiate any necessary corrective action. Critical process steps are 100% under statistical process control.
- Acceptance tests on finished products to verify conformance with the device specification. The test results are used for quality feedback and corrective actions. The inspection and test requirements are detailed in the general quality specifications.
- Periodic inspections to monitor and measure the conformance of products.

PRODUCT RELIABILITY

With the increasing complexity of Original Equipment Manufacturer (OEM) equipment, component reliability must be extremely high. Our research laboratories and development departments study the failure mechanisms of semiconductors. Their studies result in design rules and process optimization for the highest built-in product reliability. Highly accelerated tests are applied to the products reliability evaluation. Rejects from reliability tests and from customer complaints are submitted to failure analysis, to result in corrective action.

CUSTOMER RESPONSES

Our quality improvement depends on joint action with our customer. We need our customer's inputs and we invite constructive comments on all aspects of our performance. Please contact our local sales representative.

RECOGNITION

The high quality of our products and services is demonstrated by many Quality Awards granted by major customers and international organizations.

BASIC TYPE NUMBER

This type designation code applies to semiconductor monolithic, semiconductor multi-chip, thin film, thick film and hybrid integrated circuits. The basic type number comprises three letters followed by a serial number.

First and second letters

DIGITAL FAMILY CIRCUITS

The first two letters identify the family.(1)

SOLITARY CIRCUITS

The first letter divides solitary circuits into:

S Solitary digital circuits

T Analog circuits

U Mixed analog/digital circuits.

The second letter is a serial letter without any further significance except 'H' which stands for hybrid circuits.(2)

MICROPROCESSORS

The first two letters identify microprocessors and related circuits:

MA Microcomputer or central processing unit

MB Slice processor (functional slice of microprocessor)

MD Related memories

ME Other related circuits such as interfaces, clocks, peripheral controllers, etc.

CHARGE-TRANSFER DEVICES AND SWITCHED CAPACITORS

The first two letters identify:

NH Hybrid circuits

NL Logic circuits

NM Memories

NS Analog signal processing using switched capacitors

NT Analog signal processing using charge-transfer devices

NX Imaging devices

NY Other related circuits.

(1) A logic family is an assembly of digital circuits designed to be interconnected and defined by its base electrical characteristics, such as supply voltage, power consumption, propagation delay, noise immunity.

(2) The first letter 'S' should be used for all solitary memories, to which, in the event of hybrids, the second letter 'H' should be added, for example, SH for bubble memories.

Third letter

The third letter indicates the operating ambient temperature range:

A temperature range not specified below

B 0 to +70 °C

C −55 to +125 °C

D −25 to +70 °C

E −25 to +85 °C

F −40 to +85 °C

G −55 to +85 °C.

If a device has another temperature range, the letter 'A' or a letter indicating a narrower temperature may be used, for example, the range of 0 to +75 °C can be indicated by 'A' or 'B'. Should two devices with the same basic type number both have temperature ranges other than those specified, one would use the letter 'A' and the other the letter 'X'.

SERIAL NUMBER

This may be a four-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

VERSION LETTER

A single version letter may be added to the basic type number. This indicates a minor variant of the basic type or the package. The version letter has no fixed meaning except for 'Z' which means customized wiring. The following letters are recommended for package variants:

C Cylindrical

D Ceramic dual in-line (CERDIL, CERDIP)

F Flat pack (two leads)

G Flat pack (four leads)

H Quad flat pack (QFP)

L Chip on tape (foil)

P Plastic dual in-line (DIL)

Q Quad in-line (QUIL)

T Mini pack (SOL, SO, VSO)

U Uncased chip.

TWO-LETTER SUFFIX

A two-letter suffix may be used instead of a single package version letter to give more information. To avoid confusion with serial numbers that end with a letter, a hyphen should precede the suffix.

First letter (general shape)

C Cylindrical
D Dual in-line (DIL)
E Power DIL (with external heatsink)
F Flat pack (leads on two sides)
G Flat pack (leads on four sides)
H Quad flat pack (QFP)
K Diamond (TO-3 family)
M Multiple in-line (except dual, triple and quad)
Q Quad in-line (QUIL)
R Power QUIL (with external heatsink)
S Single in-line (SIL)
T Triple in-line
W Leaded chip carrier (LCC)
X Leadless chip carrier (LLCC)
Y Pin grid array (PGA).

Second letter (material)

C Metal-ceramic
G Glass-ceramic
M Metal
P Plastic.

EXAMPLES

PCF1105WP: digital IC; PC family; operating temperature range −40 to +85 °C; serial number 1105; plastic leaded chip carrier.

GMB74LS00A-DC: digital IC; GM family; operating temperature range 0 to +70 °C; company number 74LS00A; ceramic DIL package.

TDA1000P: analog IC; operating temperature range non-standard; serial number 1000; plastic DIL package.

SAC2000: solitary digital circuit; operating temperature range −55 to +125 °C; serial number 2000.

RATING SYSTEMS

The rating systems described are those recommended by the IEC in its publication number 134.

Definitions of terms used

ELECTRONIC DEVICE

An electronic tube or valve, transistor or other semiconductor device. This definition excludes inductors, capacitors, resistors and similar components.

CHARACTERISTIC

A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

BOGEY ELECTRONIC DEVICE

An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics that are directly related to the application.

RATING

A value that establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms. Limiting conditions may be either maxima or minima.

RATING SYSTEM

The set of principles upon which ratings are established and which determine their interpretation. The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

Absolute maximum rating system

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type, as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout the life of the device, no absolute maximum value for the intended service is exceeded with any device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

Design maximum rating system

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout the life of the device, no design maximum value for the intended service is exceeded with a bogey electronic device, under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

Design centre rating system

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

General

Rating systems

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

ELECTROSTATIC CHARGES

Electrostatic charges can exist in many things; for example, man-made-fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depend on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of the surrounding air.

Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All of our MOS devices are internally protected against electrostatic discharge but they **can** be damaged if the following precautions are not taken.

WORK STATION

Figure 1 shows a working area suitable for safely handling electrostatic sensitive devices. It has a work bench, the surface of which is conductive or covered by an antistatic sheet. Typical resistivity for the bench surface is between 1 and 500 kΩ per cm^2. The floor should also be covered with antistatic material. The following precautions should be observed:

- Persons at a work bench should be earthed via a wrist strap and a resistor.
- All mains-powered electrical equipment should be connected via an earth leakage switch.
- Equipment cases should be earthed.
- Relative humidity should be maintained between 50 and 65%.
- An ionizer should be used to neutralize objects with immobile static charges.

RECEIPT AND STORAGE

MOS devices are packed for dispatch in antistatic/conductive containers, usually boxes, tubes or blister tape. The fact that the contents are sensitive to electrostatic discharge is shown by warning labels on both primary and secondary packing.

The devices should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be performed at a protected work station. Any MOS devices that are stored temporarily should be packed in conductive or antistatic packing or carriers.

ASSEMBLY

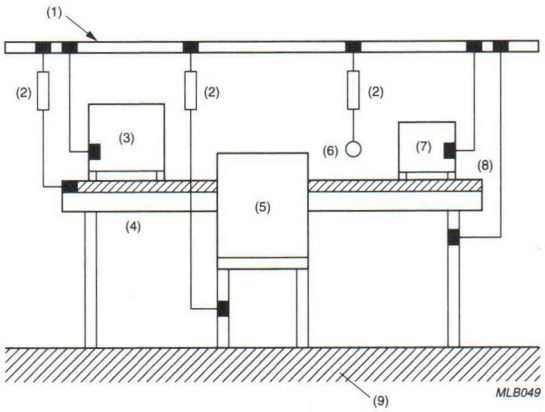
MOS devices must be removed from their protective packing with earthed component pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Do not remove more devices from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken.

During assembly, ensure that the MOS devices are the last of the components to be mounted and that this is done at a protected work station.

All tools used during assembly, including soldering tools and solder baths, must be earthed. All hand tools should be of conductive or antistatic material and, where possible, should not be insulated.

Measuring and testing of completed circuit boards must be done at a protected work station. Place the soldered side of the circuit board on conductive or antistatic foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board does not touch the conductive surface of the work bench. After testing, replace the circuit board on the conductive foam to await packing.

Assembled circuit boards containing MOS devices should be handled in the same way as unmounted MOS devices. They should also carry warning labels and be packed in conductive or antistatic packing.



(1) Earthing rail.
(2) Resistor (500 kΩ ± 10%, 0.5 W).
(3) Ionizer.
(4) Work bench.
(5) Chair.
(6) Wrist strap.
(7) Electrical equipment.
(8) Conductive surface/antistatic sheet.
(9) Antistatic floor.

Fig.1 Protected work station.

DEVICE DATA

(in alphanumeric sequence)

32 kHz watch circuits with adaptive motor pulse

PCA146x series

FEATURES

- 32 kHz oscillator, amplitude regulated with excellent frequency stability
- High immunity of the oscillator to leakage currents
- Time calibration electrically programmable and reprogrammable (via EEPROM)
- A quartz crystal is the only external component required
- Very low current consumption; typically 170 nA
- Output for bipolar stepping motors of different types
- Up to 50% reduction in motor current compared with conventional circuits, by self adaption of the motor pulse width to match the required torque of the motor
- No loss of motor steps possible because of on-chip detection of the induced motor voltage
- Detector for lithium or silver-oxide battery voltage levels
- Indication for battery end-of-life
- Stop function for accurate timing
- Power-on reset for fast testing
- Various test modes for testing the mechanical parts of the watch and the IC.

GENERAL DESCRIPTION

The PCA146x series devices are CMOS integrated circuits specially suited for battery-operated, quartz-crystal-controlled wrist-watches, with a bipolar stepping motor.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE[1]		
	NAME	DESCRIPTION	VERSION
PCA1461U	–	chip in tray	–
PCA1461U/10	–	chip on foil	–
PCA1462U	–	chip in tray	–
PCA1462U/7	–	chip with bumps on tape	–
PCA1462U/10	–	chip on foil	–
PCA1463U	–	chip in tray	–
PCA1463U/10	–	chip on foil	–
PCA1465U/10	–	chip on foil	–
PCA1465U/7	–	chip with bumps on tape	–
PCA1467U/10	–	chip on foil	–

Note

1. Figure 1 and Chapter "Package outline" show details of standard package, available for large orders only. Chapter "Chip dimensions and bonding pad locations" shows exact pad locations for other delivery formats.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{SS}	1	ground (0 V)
TEST	2	test output
OSC IN	3	oscillator input
OSC OUT	4	oscillator output
V_{DD}	5	supply voltage
M1	6	motor 1 output
M2	7	motor 2 output
RESET	8	reset input

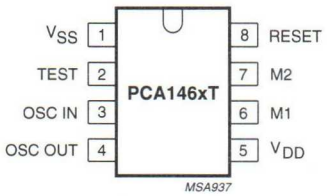


Fig.1 Pin configuration, PCA146xT, (PMFP8).

FUNCTIONAL DESCRIPTION AND TESTING

The motor output delivers pulses of six different stages depending on the torque required to turn the motor (Figs. 3 and 4). Every motor pulse is followed by a detection phase which monitors the waveform of the induced motor voltage. When a step is missed a correction sequence will be started (Fig.2).

Motor pulses

The circuit produces motor pulses of six different stages (stage 1 to 5, stage 8). Each stage has two independent modes: silver-oxide and lithium. The voltage level of V_{DD} determines which mode is selected (see Section "Voltage level detector").

Stages 1 to 5 (both modes) are used in normal operation, stage 8 occurs under the following conditions:

- Correction pulse after a missing step (both modes)
- End-of-life mode
- If stage 5 is not enough to turn the motor (both modes).

In the silver-oxide mode, the ON state of the motor pulse varies between 56.25% and 100% of the duty factor t_{DF} = 977 µs depending on the stage (Fig.3). It increases in steps of 6.25% per stage.

In the lithium mode, the ON state of the motor pulse is reduced by 18.75% of the duty factor t_{DF} (Fig.4) to compensate for the increase in the voltage level.

After a RESET the circuit always starts and continues with stage 1, when all motor pulses have been executed. A failure to execute all motor pulses results in the circuit going into stage 2, this sequence will be repeated through to stage 8.

When the motor pulses at stage 5 are not large enough to turn the motor, stage 8 is implemented for a maximum of 8 minutes with no attempt to keep current consumption low. After stage 8 has been executed the procedure is repeated from RESET.

The circuit operates for 8 minutes at a fixed stage, if every motor pulse is executed. The next 480 motor pulses are then produced at the next lower stage unless a missing step is detected. If a step is missed a correction sequence is produced and for a maximum of 8 minutes the motor pulses are increased by one stage.

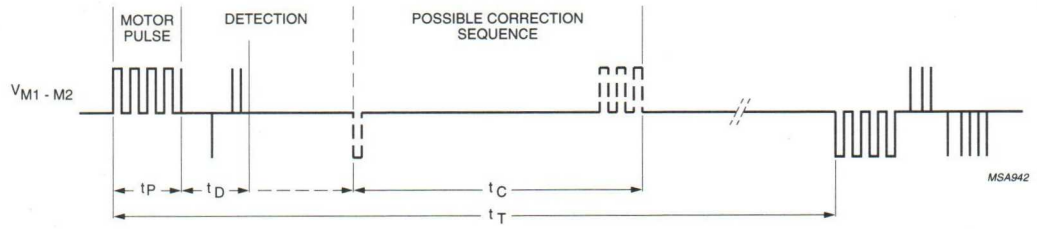
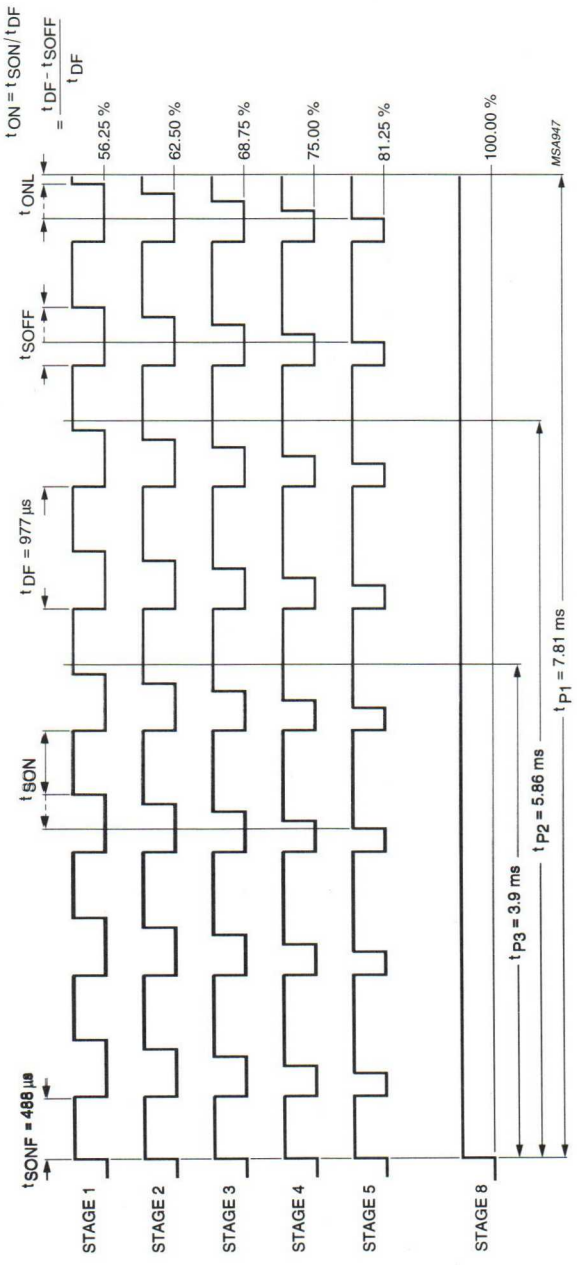


Fig.2 Possible motor output waveform in normal operation with motor connected.



t_{OFF} for stage 1 to 5 = 488 µs − stage × 61 µs
t_{ON} for stage 1 to 5 = 488 µs + stage × 61 µs

Fig.3 Motor pulses in the silver-oxide mode (V_{DD} = 1.55 V).

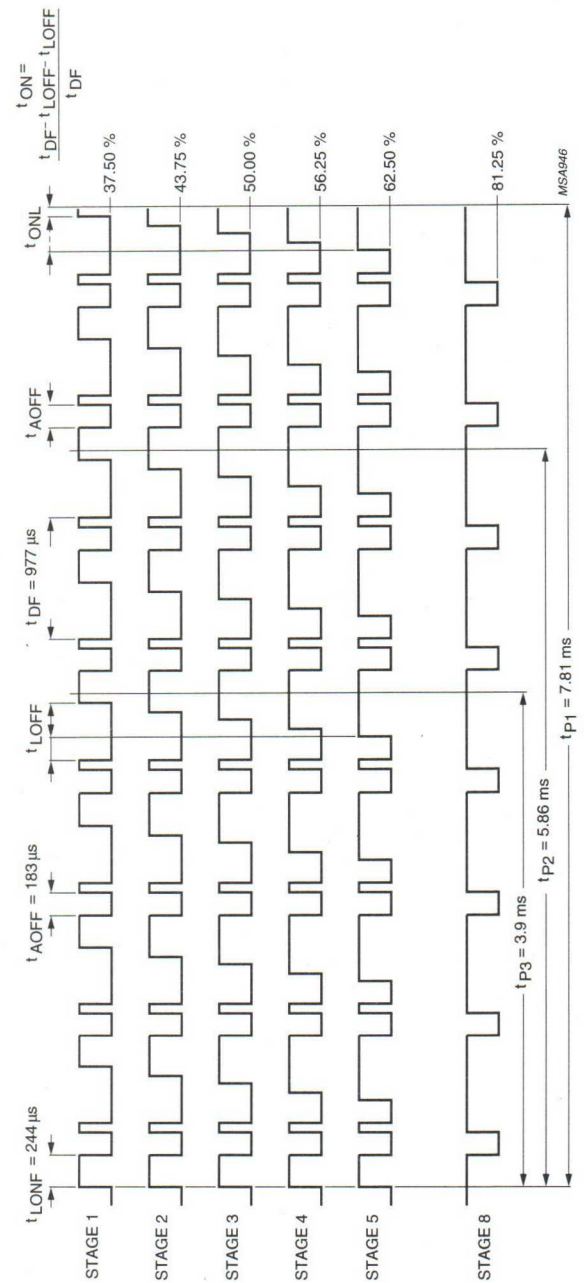


Fig.4 Motor pulses in the lithium mode (V_{DD} = 2.1 V).

t_{OFF} for stage 1 to 5 = 672 µs − stage × 61 µs
t_{ON} for stage 1 to 5 = 305 µs + stage × 61 µs

Voltage level detector

The supply voltage is compared with the internal voltage reference V_{LIT} and V_{EOL} every minute. The first voltage level detection is carried out 30 ms after RESET.

When a lithium voltage level is detected ($V_{DD} \geq V_{LIT}$), the circuit starts operating in the lithium mode (Fig.4).

When the detected V_{DD} voltage level is between V_{LIT} and V_{EOL}, the circuit operates in the silver-oxide mode (Fig.3).

If the battery end-of-life is detected ($V_{DD} < V_{EOL}$), the detection and stage control is switched OFF and the waveform produced is an unchopped version of the stage 8 waveform. To indicate this condition the waveform is produced in bursts of 4 pulses every 4 s.

Detection of motor movement

After a motor pulse, the motor is short-circuited to V_{DD} for 1 ms. Afterwards the energy in the motor inductor will be dissipated to measure only the current generated by the induced motor voltage. During the time t_{DI} (dissipation of energy time) all switches shown in Fig.5 are open to reduce the current as fast as possible. The current will now flow through the diodes D3 and D2, or D4 and D1. Then the first of 52 possible measurement cycles (t_{MC}) starts to measure the induced current.

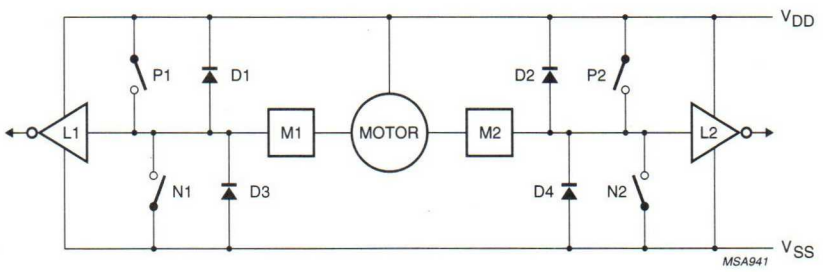


Fig.5 Motor driving and detecting circuit.

Detection criteria

The PCA146x uses current detection in two defined parts of the detection phase to determine if the motor has moved (refer to Figs 6 and 7). The detection criteria are:

part 1

- Minimum value of P = 1; where P = number of measured positive current polarities after t_{DI}.

part 2

- Minimum value of N = 2; where N = number of measured positive current polarities since the first negative current polarity after part 1 was detected (see Fig.6).

If the opposite polarity is measured in one part, the internal counter is reset, so the results of all measurements in this part are ignored.

The waveform of the induced current must enable all these measurements within the time t_D after the end of a positive motor pulse in order to be accepted as a waveform of an executed motor pulse.

If the detection criterion is satisfied earlier, a measurement cycle will not be started and the switches P1 and P2 stay closed, the motor is switched to V_{DD}.

Every measurement cycle (t_{MC}) has 4 phases. These are detailed in Table 1.

Note that detection and pulse width control will be switched OFF when the battery voltage is below the end-of-life voltage (V_{EOL}), or if stage 5 is not sufficient to turn the motor.

Table 1 Measurement cycle

SYMBOL	PHASE	DESCRIPTION
t_{M1}	1	During t_{M1} the switches P1 and P2 are closed in order to switch the motor to V_{DD}, so the induced current flows unaffected through the motor inductance.
t_{M2}	2	Measures the induced current; during a maximum time t_{M2} all switches are open until a change is sensed by one of the level detectors (L1, L2). The motor is short-circuited to V_{DD}. Depending on the direction of the interrupted current: • The current flows through diodes D3 and D2, causing the voltage at M1 to decrease in relation to M2; • The current flows through diodes D4 and D1, causing the voltage at M2 to decrease in relation to M1. A successfully detected current polarity is normally characterized by a short pulse of 0.5 to 10 µs with a voltage up to ±2.1 V, failed polarity detection by the maximum pulse width of 61 µs and a voltage of ±0.5 V (see Fig.7).
t_{M3}	3	The switches P1 and P2 remain closed for the time t_{M3}.
t_{M4}	4	If the circuit detects fewer pulses than P and N respectively, a pulse of the time t_{M4} occurs to reduce the induced current. Therefore P2 and P1 are opened and N1 and N2 are closed. Otherwise P1 and P2 remain closed.

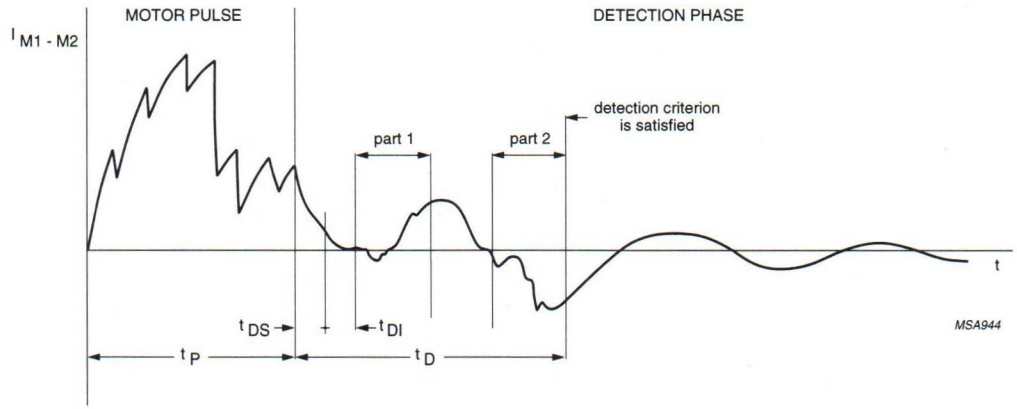


Fig.6 Typical current waveform of a successfully executed motor pulse.

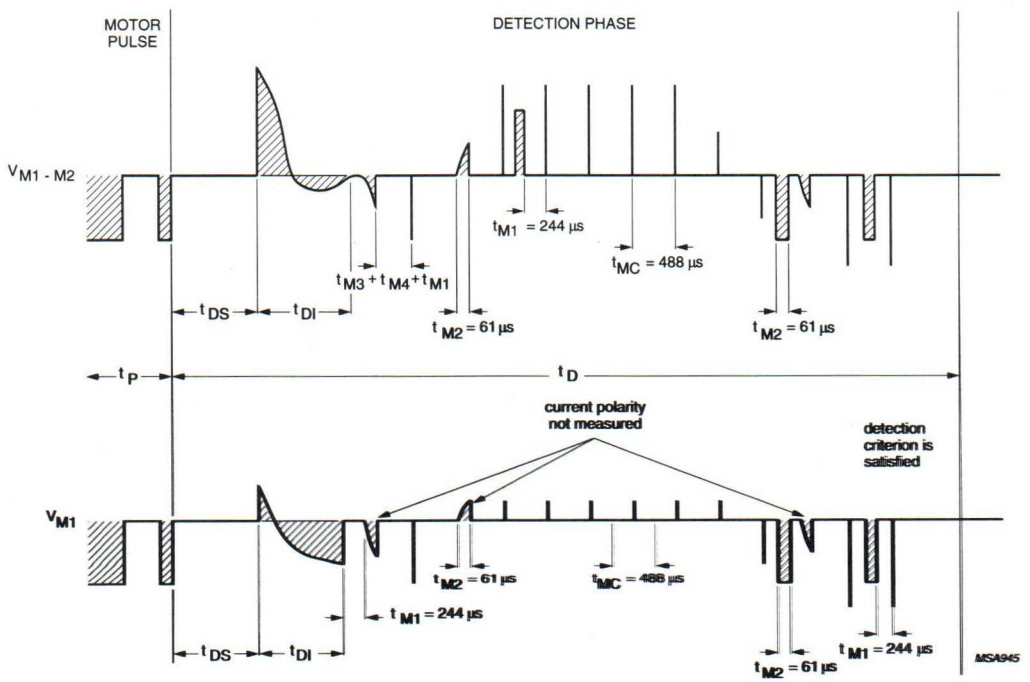


Fig.7 Detection phase of the current waveform in Fig.6.

Correction sequence (see Fig.8)

If a missing step is detected, a correction sequence is produced. This consists of a small pulse (t_{C1}) which gives the motor a defined position and after 29.30 ms a pulse of stage 8 (t_{C2}) to turn the motor.

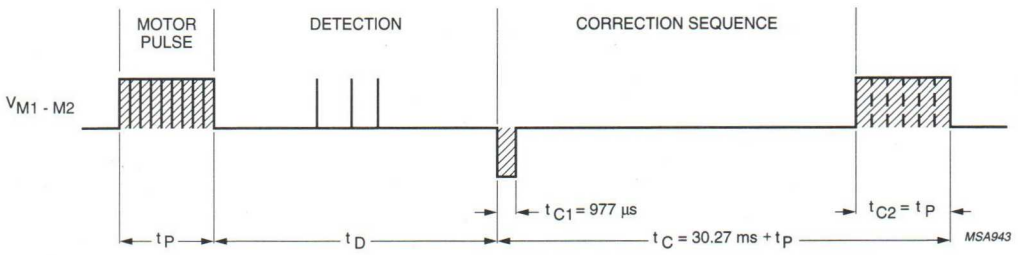


Fig.8 Correction sequence after a missing motor step with motor connected.

Time calibration

Taking a normal quartz crystal with frequency 32768kHz, frequency deviation ($\Delta f/f$) of $\pm 15 \times 10^{-6}$ and C_L = 8.2 pF; the oscillator frequency is offset (by using non-symmetrical internal oscillator input and output capacitances of 10 pF and 15 pF) such that the frequency deviation is positive-only. This positive deviation can then be compensated for to maintain time-keeping accuracy.

Once the positive frequency deviation is measured, a corresponding number 'n' (see Table 2) can be programmed into the device's EEPROM. This causes n pulses of frequency 8192 Hz to be inhibited every minute of operation, which achieves the required calibration.

The programming circuit is shown in Fig.9. The required number n is programmed into EEPROM by varying V_{DD} according to the steps shown in Fig.10, which are explained below:

1. The positive quartz frequency deviation ($\Delta f/f$) is measured, and the corresponding values of n are found according to Table 2.
2. V_{DD} is increased to 5.1 V allowing the contents of the EEPROM to be checked from the motor pulse period t_{T3} at nominal frequency.
3. V_{DD} is decreased to 2.5 V during a motor pulse to initialize a storing sequence.
4. The first V_{DD} pulse to 5.1 V erases the contents of EEPROM.
5. When the EEPROM is erased a logic 1 is at the TEST pin.
6. V_{DD} is increased to 5.1 V to read the data by pulsing V_{DD} n times to 4.5 V. After the n edge, V_{DD} is decreased to 2.5 V.
7. V_{DD} is increased to 5.1 V to store n bits in the EEPROM.
8. V_{DD} is decreased to 2.5 V to terminate the storing sequence and to return to operating mode.
9. V_{DD} is increased to 5.1 V to check writing from the motor pulse period t_{T3}.
10. V_{DD} is decreased to the operation voltage **between** two motor pulses to return to operating mode. (Decreasing V_{DD} during the motor pulse would restart the programming mode).

The time calibration can be reprogrammed up to 100 times.

Table 2 Quartz crystal frequency deviation, n and t_{T3}

FREQUENCY DEVIATION $\Delta f/f$ ($\times 10^{-6}$)	NUMBER OF PULSES (n)	t_{T3} (ms)
0[1]	0	31.250[2]
+2.03	1	31.372
+4.06	2	31.494
.	.	.
.	.	.
.	.	.
+127.89	63	38.936

Notes

1. Increments of 2.03×10^{-6}/step.
2. Increments of 122 µs/step.

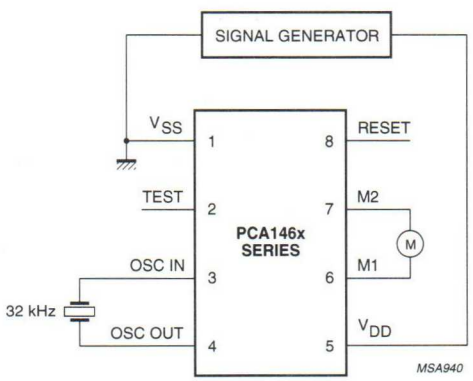


Fig.9 Circuit for programming the time calibration.

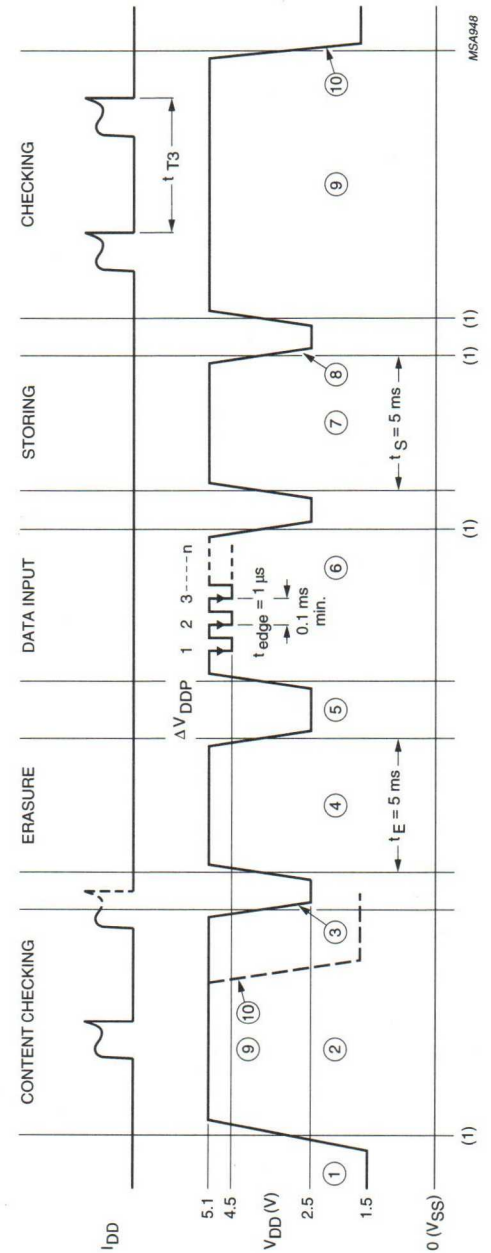


Fig.10 V_{DD} for programming.

(1) Rise and fall time should be greater than 400 µs/V for immediately correct checking.

Power-on reset

For correct operation of the Power-on reset the rise time of V_{DD} from 0 V to 2.1 V should be less than 0.1 ms.
All resetable flip-flops are reset. Additionally the polarity of the first motor pulse is positive: $V_{M1} - V_{M2} \geq 0$ V.

Customer testing

An output frequency of 32 Hz is provided at RESET (pin 8) to be used for exact frequency measurement. Every minute a jitter occurs as a result of the inhibition, which occurs 90 to 150 ms after disconnecting the RESET from V_{DD}.

Connecting the RESET to V_{DD} stops the motor pulses leaving them in a 3-state mode and sets the motor pulse width for the next available motor pulse to stage 1 in the silver-oxide mode. A 32 Hz signal without jitter is produced at the TEST pin.
Debounce time RESET = 14.7 to 123.2 ms.

Connecting RESET to V_{SS} activates Tests 1 and 2 and disables the inhibition.

Test 1, $V_{DD} > V_{EOL}$. Normal function takes place except that the motor pulse period is t_{T1} = 125 ms instead of t_T, and the motor pulse stage is reduced every second instead of every 8 minutes. At TEST a speeded-up 8 minute signal is available.

Test 2, $V_{DD} < V_{EOL}$. Motor pulses of stage 8 are produced, with a time period of t_{T2} = 31.25 ms.

Test and reset modes are terminated by disconnecting the RESET pin.

Test 3, $V_{DD} > 5.1$ V. Motor pulses of stage 8 are produced, with a time period of t_{T3} = 31.25 ms and $n \times 122$ µs to check the contents of the EEPROM. At TEST a speeded-up cycle for motor pulse period signal t_T is available at 1024 times its normal frequency.
Decreasing V_{DD} voltage level to lower than 2.5 V between two motor pulses returns the circuit to normal operating conditions.

AVAILABLE TYPES

Refer to Chapters "Ordering information" and "Functional description and testing".

SHORT TYPE NUMBER	DELIVERY FORMAT[1]	PERIOD t_T (s)	SPECIFICATIONS					
			PULSE WIDTH t_P (ms)	DRIVE (%)	DETECTION CRITERION	EEPROM	BATTERY EOL DETECTION	REMARKS
1461	U; U/10	1	7.8	max. 100 81	P = 1 N = 2	yes	yes	1.5 V and 2.1 V Lithium
1462	U; U/7; U/10	1	5.8	max. 100 81	P = 1 N = 2	yes	yes	1.5 V and 2.1 V Lithium
1463	U; U/10	1	3.9	max. 100 81	P = 1 N = 2	yes	yes	1.5 V and 2.1 V Lithium
1465	U/10; U/7	1	5.8	max. 100	P = 1 N = 2	yes	no	1.5 V
1467	U/10	1	7.8	max. 100	P = 1 N = 2	yes	no	1.5 V

Note

1. U = Chip in tray; U/7 = chip with bumps on tape; U/10 = chip on foil.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	V_{SS} = 0 V; note 1	−1.8	+6	V
V_I	all input voltages		V_{SS}	V_{DD}	V
	output short-circuit duration			indefinite	
T_{amb}	operating ambient temperature		−10	+60	°C
T_{stg}	storage temperature		−30	+100	°C

Note

1. Connecting the battery with reversed polarity does not destroy the circuit, but in this condition a large current flows, which will rapidly discharge the battery.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advisable to take handling precautions appropriate to handling MOS devices. Advice can be found in *"Data Handbook IC16, General, Handling MOS Devices"*.

CHARACTERISTICS

V_{DD} = 1.55 V; V_{SS} = 0 V; f_{osc} = 32.768 kHz; T_{amb} = 25 °C; crystal: R_S = 20 kΩ; C_1 = 2 to 3 fF; C_L = 8 to 10 pF; C_0 = 1 to 3 pF; unless otherwise specified.

Immunity against parasitic impedance = 20 MΩ between adjacent pins.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD1}	supply voltage	T_{amb} = −10 to +60 °C	1.2	1.55	2.5	V
ΔV_{DD}	supply voltage variation	transient within 1.2 V and 2.5 V	–	–	0.25	V
V_{DD2}	supply voltage	programming	5.0	5.1	5.2	V
ΔV_{DDP}	supply voltage pulse variation	programming	0.55	0.6	0.65	V
I_{DD1}	supply current	between motor pulses	–	170	260	nA
I_{DD2}	supply current	V_{DD} = 2.1 V	–	190	300	nA
I_{DD3}	supply current	stop mode; pin 8 connected to V_{DD}	–	180	280	nA
I_{DD4}	supply current	V_{DD} = 2.1 V	–	220	360	nA
I_{DD5}	supply current	T_{amb} = −10 to +60 °C	–	–	600	nA
Motor output						
V_{sat}	saturation voltage Σ (P + N)	R_M = 2 kΩ; T_{amb} = −10 to +60 °C	–	150	200	mV
$Z_{o(sc)}$	output short-circuit impedance	between motor pulses $I_{transistor}$ < 1 mA	–	200	300	Ω

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator						
$V_{OSC\ ST}$	starting voltage		1.2	–	–	V
g_m	transconductance	$V_{i(p-p)} \leq 50$ mV	6	15	–	µS
t_{osc}	start-up time		–	1	–	s
$\Delta f/f$	frequency stability	$\Delta V_{DD} = 100$ mV	–	0.05×10^{-6}	0.3×10^{-6}	
C_i	input capacitance		8	10	12	pF
C_o	output capacitance		12	15	18	pF
Voltage level detector						
V_{LIT}	threshold voltage		1.62	1.80	1.98	V
V_{EOL}	threshold voltage		1.30	1.38	1.46	V
ΔV_{EOL}	hysteresis of threshold		–	10	–	mV
TC_{EOL}	temperature coefficient		–	–1	–	mV/K
Reset input						
f_o	output frequency		–	32	–	Hz
ΔV_o	output voltage swing	R = 1 MΩ; C = 10 pF	1.4	–	–	V
t_{edge}	edge time	R = 1 MΩ; C = 10 pF	–	1	–	µs
I_{im}	peak input current	note 1	–	320	–	nA
$I_{i(av)}$	average input current		–	10	–	nA

Note

1. Duty factor is 1 : 32 and RESET = V_{DD} or V_{SS}.

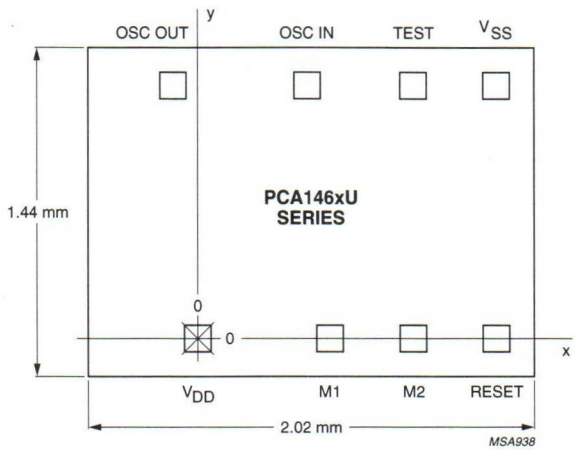
TIMING PARAMETERS

SYMBOL	PARAMETER	SECTION	VALUE	OPTION	UNIT
t_T	cycle for motor pulse (note 1)	motor pulse (Figs 2, 3 and 4)	1	5, 10, 12 or 20	s
t_P	motor pulse width		7.81	3.9 or 5.9	ms
t_{DF}	duty factor		977	–	µs
t_{ONL}	last duty factor on		61 to 305	–	µs
t_v	voltage detection cycle	level mode	60	–	s
t_{SON}	duty factor on	silver-oxide mode (Fig.3)	550 to 794	–	µs
t_{SOFF}	duty factor off		427 to 183	–	µs
t_{SONF}	first duty factor on		488	–	µs
t_{AOFF}	additional duty factor off	lithium mode (Fig.4)	183	–	µs
t_{LON}	duty factor on		305 to 611	–	µs
t_{LOFF}	duty factor off		672 to 366	–	µs
t_{LONF}	first duty factor on		244	–	µs
t_E	EOL sequence	end-of-life mode	4	–	s
t_{E1}	motor pulse width		t_P	–	ms
t_{E2}	time between pulses		31.25	–	ms
t_D	detection sequence	detection (Fig.7)	4.3 to 28.3	–	ms
t_{DS}	short-circuited motor		977	–	µs
t_{DI}	dissipation of energy		977	–	µs
t_{MC}	measurement cycle		488	–	µs
t_{M1}	phase 1		244	–	µs
t_{M2}	phase 2 (measure window)		61	–	µs
t_{M3}	phase 3		122	–	µs
t_{M4}	phase 4		61	–	µs
P	positive current polarities		1	P < N	
N	negative current polarities		2	2 to 6	
t_C	correction sequence	correction sequence (Fig.8)	t_P + 30.27	–	ms
t_{C1}	small pulse width		977	–	µs
t_{C2}	large pulse width		t_P	–	ms
	cycles for motor-pulses in:	testing			
t_{T1}	test 1		125	–	ms
t_{T2}	test 2		31.25	–	ms
t_{T3}	test 3	Fig.10	31.25 to 39	–	ms
t_{DEB}	debounce time for RESET = V_{DD}		14.7 to 123.2	–	ms

Note

1. No option available when EOL indication is required.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



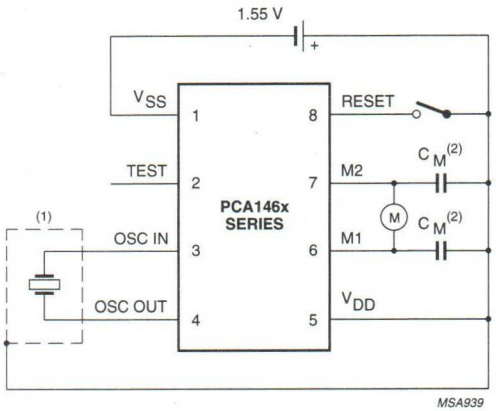
Chip area: 2.91 mm^2.
Bonding pad dimensions: 110 µm × 110 µm.
Chip thickness: 200 ±25 µm, with bumps: 270 ±25 µm.

Fig.11 Bonding pad locations, PCA146xU series; 8 terminals.

Table 3 Bonding pad locations (dimensions in µm)
All x/y coordinates are referenced to bottom left pad (V_{DD}), see Fig.11.

PAD	x	y
V_{SS}	1290	1100
TEST	940	1100
OSC IN	481	1100
OSC OUT	−102	1100
V_{DD}	0	0
M1	578	0
M2	930	0
RESET	1290	0
chip corner (max. value)	−497.5	−170

APPLICATION INFORMATION



(1) Quartz crystal case should be connected to V_{DD}. Stray capacitance and leakage resistance from RESET, M1 or M2 to OSC IN should be less than 0.5 pF or larger than 20 MΩ.

(2) Motor, probe and stray capacitance from M2 or M1 to V_{DD} or V_{SS} should be less than C_M = 80 pF for correct operation of the detection circuit. Driving the motor at its minimum energy, probe and stray capacitance must be avoided.

Fig.12 Typical application circuit diagram.

32 kHz watch circuits with adaptive motor pulse

PCA148x series

FEATURES

- 32 kHz oscillator, amplitude regulated with excellent frequency stability
- High immunity of the oscillator to leakage currents
- Time calibration electrically programmable and reprogrammable (via EEPROM)
- A quartz crystal is the only external component required
- Very low current consumption; typically 170 nA
- Output for bipolar stepping motors of different types
- Up to 50% reduction in motor current compared with conventional circuits, by self adaption of the motor pulse width in accordance with the required torque of the motor
- No loss of motor steps possible because of on-chip detection of the induced motor voltage
- Indication for battery end-of-life
- Stop function for accurate timing
- Power-on reset for fast testing
- Various test modes for testing the mechanical parts of the watch and the IC.

GENERAL DESCRIPTION

The PCA148x series devices are CMOS integrated circuits specially suited for battery-operated, quartz-crystal-controlled wrist-watches, with a bipolar stepping motor.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE[1]		
	NAME	DESCRIPTION	VERSION
PCA1485U/7	–	chip with bumps on tape	–
PCA1486U/7	–	chip with bumps on tape	–
PCA1486U/10	–	chip on foil	–
PCA1487U/10	–	chip on foil	–

Note

1. Figure 1 and Chapter "Package outline" show details of standard package, available for large orders only. Chapter "Chip dimensions and bonding pad locations" shows exact pad locations for other delivery formats.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{SS}	1	ground (0 V)
TEST	2	test output
OSC IN	3	oscillator input
OSC OUT	4	oscillator output
V_{DD}	5	supply voltage
M1	6	motor 1 output
M2	7	motor 2 output
RESET	8	reset input

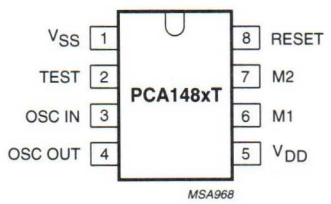


Fig.1 Pin configuration, PCA148xT, (PMFP8).

FUNCTIONAL DESCRIPTION AND TESTING

The motor output delivers pulses of six different stages depending on the torque required to turn the motor (Fig.3). Every motor pulse is followed by a detection phase which monitors the waveform of the induced motor voltage. When a step is missed a correction sequence will be started (Fig.2).

Motor pulses

The circuit produces motor pulses of six different stages (stage 1 to 5, stage 6).

Stages 1 to 5 are used in normal operation, stage 6 occurs under the following conditions:

- Correction pulse after a missing step
- End-of-life mode
- If stage 5 is not enough to turn the motor.

The ON state of the motor pulse varies between 43.75% and 75% of the duty factor t_{DF} = 977 µs depending on the stage (Fig.3). It increases in steps of 6.25% per stage.

After a RESET the circuit always starts and continues with stage 1, when all motor pulses have been executed. A failure to execute all motor pulses results in the circuit going into stage 2, this sequence will be repeated through to stage 6.

When the motor pulses at stage 5 are not large enough to turn the motor, stage 6 is implemented for a maximum of 8 minutes with no attempt to keep current consumption low. After stage 6 has been executed the procedure is repeated from RESET.

The circuit operates for 8 minutes at a fixed stage, if every motor pulse is executed. The next 480 motor pulses are then produced at the next lower stage unless a missing step is detected. If a step is missed a correction sequence is produced and for a maximum of 8 minutes the motor pulses are increased by one stage.

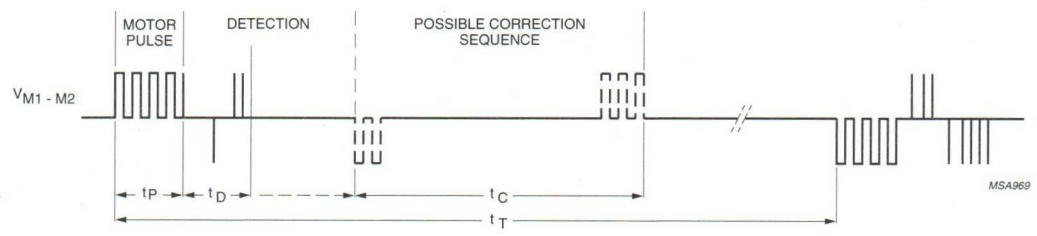
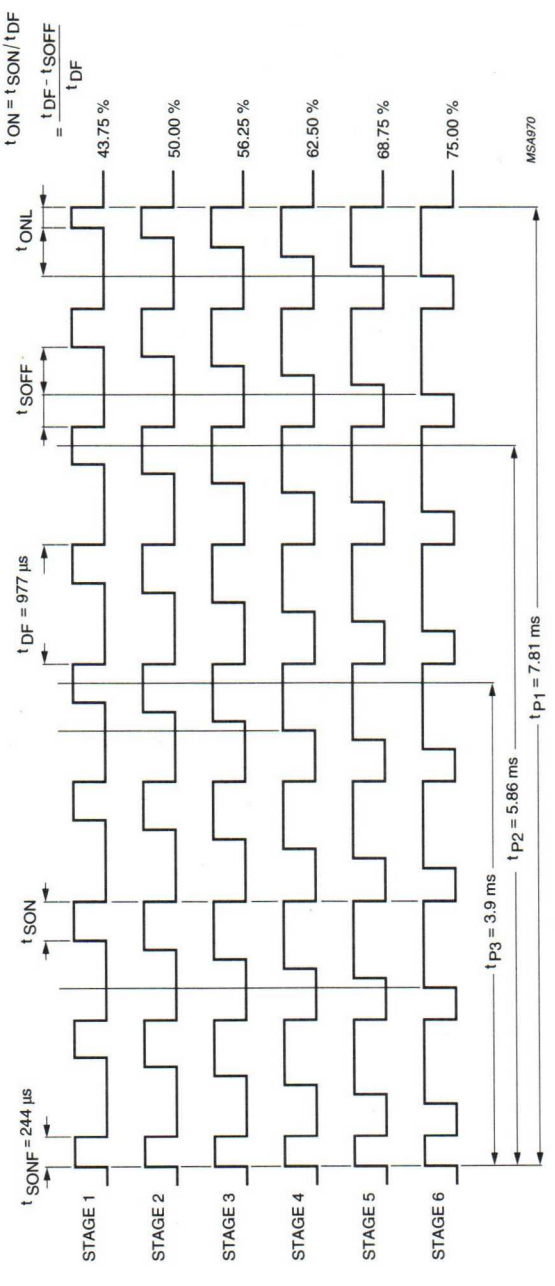


Fig.2 Possible motor output waveform in normal operation with motor connected.



t_{OFF} for stage 1 to 6 = 611 µs − stage × 61 µs
t_{ON} for stage 1 to 6 = 366 µs + stage × 61 µs

Fig.3 Motor pulses (V_{DD} = 1.55 V).

Voltage level detector

The supply voltage is compared with the internal voltage reference V_{EOL} every minute. The first voltage level detection is carried out 30 ms after RESET.

When the detected V_{DD} voltage level is greater than V_{EOL}, the circuit operates in normal mode (Fig.3).

If the battery end-of-life is detected ($V_{DD} < V_{EOL}$), the detection and stage control is switched OFF and the waveform of stage 6 will be executed. To indicate this condition the waveform is produced in bursts of 4 pulses every 4 s.

Detection of motor movement

After a motor pulse, the motor is short-circuited to V_{DD} for 1 ms. Afterwards the energy in the motor inductor will be dissipated to measure only the current generated by the induced motor voltage. During the time t_{DI} (dissipation of energy time) all switches shown in Fig.4 are open to reduce the current as fast as possible. The current will now flow through the diodes D3 and D2, or D4 and D1. Then the first of 52 possible measurement cycles (t_{MC}) starts to measure the induced current.

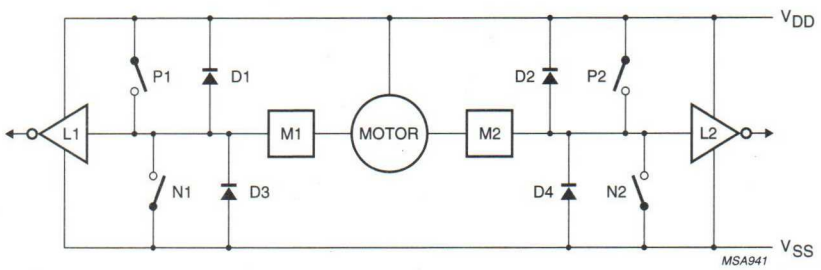


Fig.4 Motor driving and detecting circuit.

Detection criteria

The PCA148x uses current detection in two defined parts of the detection phase to determine if the motor has moved (refer to Figs 5 and 6). The detection criteria are:

part 1

- Minimum value of P = 1; where P = number of measured positive current polarities after t_{DI}.

part 2

- Minimum value of N = 2; where N = number of measured positive current polarities since the first negative current polarity after part 1 was detected (see Fig.5).

If the opposite polarity is measured in one part, the internal counter is reset, so the results of all measurements in this part are ignored.

The waveform of the induced current must enable all these measurements within the time t_D after the end of a positive motor pulse in order to be accepted as a waveform of an executed motor pulse.

If the detection criterion is satisfied earlier, a measurement cycle will not be started and the switches P1 and P2 stay closed, the motor is switched to V_{DD}.

Every measurement cycle (t_{MC}) has 4 phases. These are detailed in Table 1.

Note that detection and pulse width control will be switched OFF when the battery voltage is below the end-of-life voltage (V_{EOL}), or if stage 5 is not sufficient to turn the motor.

Table 1 Measurement cycle

SYMBOL	PHASE	DESCRIPTION
t_{M1}	1	During t_{M1} the switches P1 and P2 are closed in order to switch the motor to V_{DD}, so the induced current flows unaffected through the motor inductance.
t_{M2}	2	Measures the induced current; during a maximum time t_{M2} all switches are open until a change is sensed by one of the level detectors (L1, L2). The motor is short-circuited to V_{DD}. Depending on the direction of the interrupted current: • The current flows through diodes D3 and D2, causing the voltage at M1 to decrease in relation to M2; • The current flows through diodes D4 and D1, causing the voltage at M2 to decrease in relation to M1. A successfully detected current polarity is normally characterized by a short pulse of 0.5 to 10 µs with a voltage up to ±2.1 V, failed polarity detection by the maximum pulse width of 61 µs and a voltage of ±0.5 V (see Fig.6).
t_{M3}	3	The switches P1 and P2 remain closed for the time t_{M3}.
t_{M4}	4	If the circuit detects fewer pulses than P and N respectively, a pulse of the time t_{M4} occurs to reduce the induced current. Therefore P2 and P1 are opened and N1 and N2 are closed. Otherwise P1 and P2 remain closed.

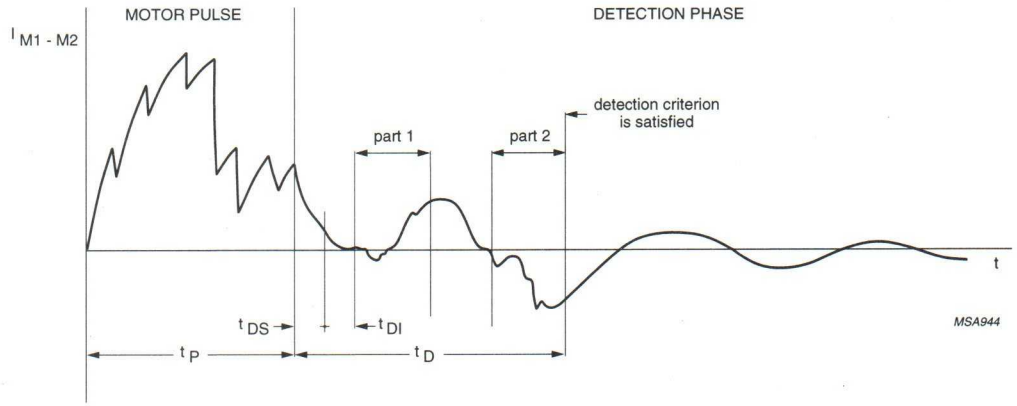


Fig.5 Typical current waveform of a successfully executed motor pulse.

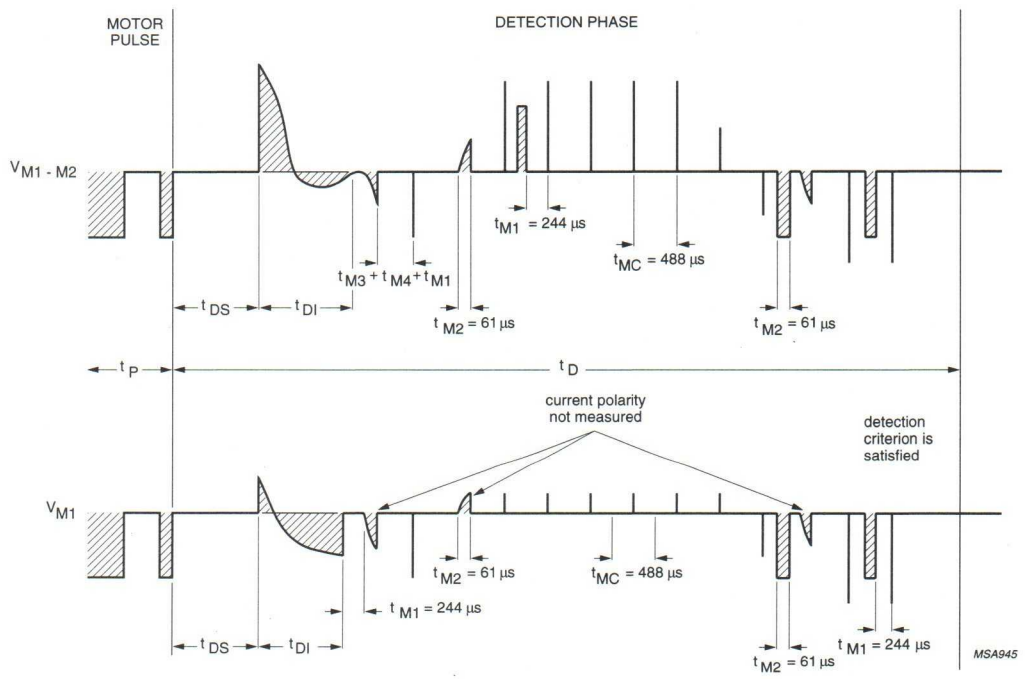


Fig.6 Detection phase of the current waveform in Fig.5.

Correction sequence (see Fig.7)

If a missing step is detected, a correction sequence is produced. This consists of a small pulse (t_{C1}) which gives the motor a defined position and after 29.30 ms a pulse of stage 6 (t_{C2}) to turn the motor.

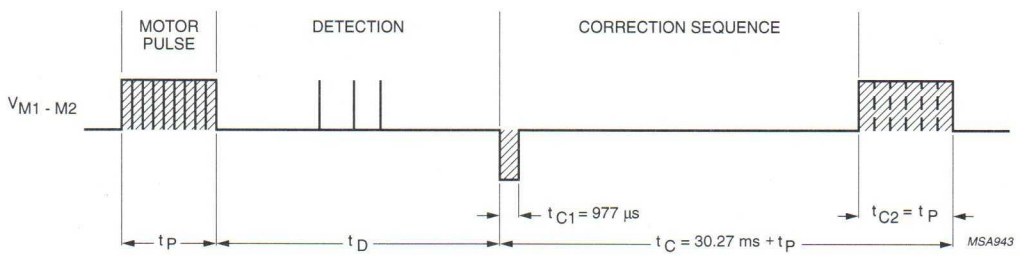


Fig.7 Correction sequence after a missing motor step with motor connected.

Time calibration

Taking a normal quartz crystal with frequency 32768kHz, frequency deviation ($\Delta f/f$) of $\pm 15 \times 10^{-6}$ and C_L = 8.2 pF; the oscillator frequency is offset (by using non-symmetrical internal oscillator input and output capacitances of 10 pF and 15 pF) such that the frequency deviation is positive-only. This positive deviation can then be compensated for to maintain time-keeping accuracy.

Once the positive frequency deviation is measured, a corresponding number 'n' (see Table 2) is programmed into the device's EEPROM. This causes n pulses of frequency 8192 Hz to be inhibited every minute of operation, which achieves the required calibration.

The programming circuit is shown in Fig.8. The required number n is programmed into EEPROM by varying V_{DD} according to the steps shown in Fig.9, which are explained below:

1. The positive quartz frequency deviation ($\Delta f/f$) is measured, and the corresponding values of n are found according to Table 2.
2. V_{DD} is increased to 5.1 V allowing the contents of the EEPROM to be checked from the motor pulse period t_{T3} at nominal frequency.
3. V_{DD} is decreased to 2.5 V during a motor pulse to initialize a storing sequence.
4. The first V_{DD} pulse to 5.1 V erases the contents of EEPROM.
5. When the EEPROM is erased a logic 1 is at the TEST pin.
6. V_{DD} is increased to 5.1 V to read the data by pulsing V_{DD} n times to 4.5 V. After the n edge, V_{DD} is decreased to 2.5 V.
7. V_{DD} is increased to 5.1 V to store n bits in the EEPROM.
8. V_{DD} is decreased to 2.5 V to terminate the storing sequence and to return to operating mode.
9. V_{DD} is increased to 5.1 V to check writing from the motor pulse period t_{T3}.
10. V_{DD} is decreased to the operation voltage **between** two motor pulses to return to operating mode. (Decreasing V_{DD} during the motor pulse would restart the programming mode).

The time calibration can be reprogrammed up to 100 times.

Table 2 Quartz crystal frequency deviation, n and t_{T3}

FREQUENCY DEVIATION $\Delta f/f$ ($\times 10^{-6}$)	NUMBER OF PULSES (n)	t_{T3} (ms)
0[1]	0	31.250[2]
+2.03	1	31.372
+4.06	2	31.494
.	.	.
.	.	.
.	.	.
+127.89	63	38.936

Notes

1. Increments of 2.03×10^{-6}/step.
2. Increments of 122 µs/step.

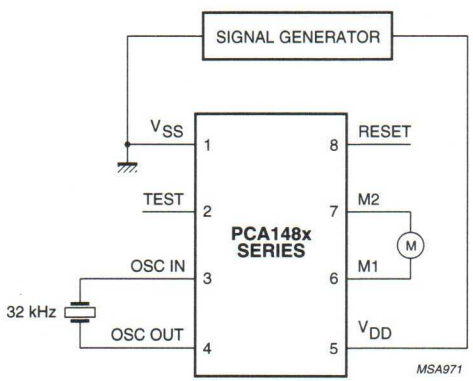


Fig.8 Circuit for programming the time calibration.

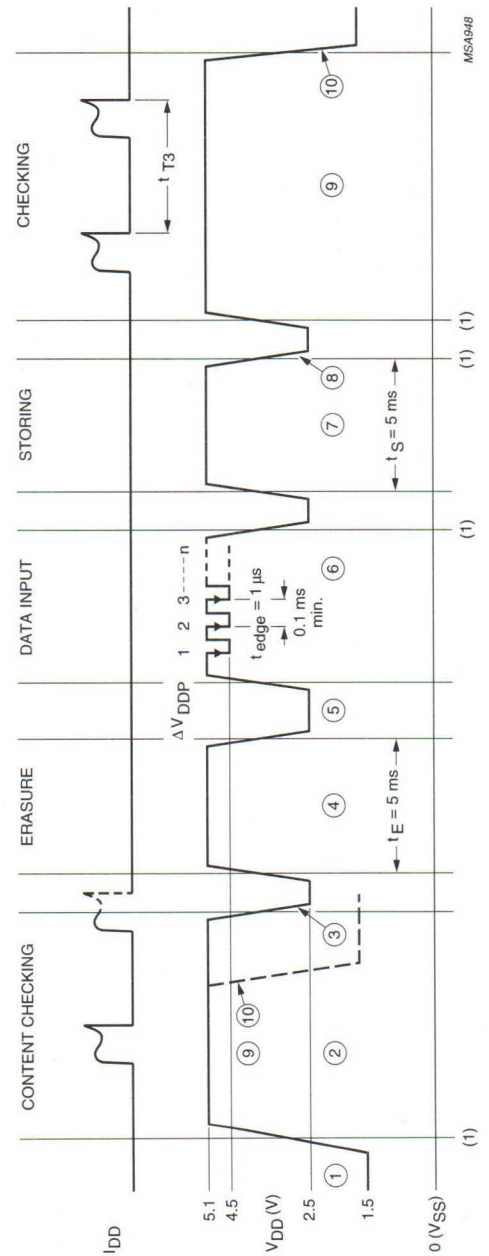


Fig.9 V_{DD} for programming.

(1) Rise and fall time should be greater than 400 µs/V for immediately correct checking.

Power-on reset

For correct operation of the Power-on reset the rise time of V_{DD} from 0 V to 2.1 V should be less than 0.1 ms. All resettable flip-flops are reset. Additionally the polarity of the first motor pulse is positive: $V_{M1} - V_{M2} \geq 0$ V.

Customer testing

An output frequency of 32 Hz is provided at RESET (pin 8) to be used for exact frequency measurement. Every minute a jitter occurs as a result of the inhibition, which occurs 90 to 150 ms after disconnecting the RESET from V_{DD}.

Connecting the RESET to V_{DD} stops the motor pulses leaving them in a 3-state mode and sets the motor pulse width for the next available motor pulse to stage 1. A 32 Hz signal without jitter is produced at the TEST pin. Debounce time RESET = 14.7 to 123.2 ms.

Connecting RESET to V_{SS} activates Tests 1 and 2 and disables the inhibition.

Test 1, $V_{DD} > V_{EOL}$. Normal function takes place except that the motor pulse period is t_{T1} = 125 ms instead of t_T, and the motor pulse stage is reduced every second instead of every 8 minutes. At TEST a speeded-up 8 minute signal is available.

Test 2, $V_{DD} < V_{EOL}$. Motor pulses of stage 6 are produced, with a time period of t_{T2} = 31.25 ms.

Test and reset modes are terminated by disconnecting the RESET pin.

Test 3, $V_{DD} > 5.1$ V. Motor pulses without chopping are produced, with a time period of t_{T3} = 31.25 ms and $n \times 122$ µs to check the contents of the EEPROM. At TEST a speeded-up cycle for motor pulse period signal t_T is available at 1 024 times its normal frequency. Decreasing V_{DD} voltage level to lower than 2.5 V between two motor pulses returns the circuit to normal operating conditions.

AVAILABLE TYPES

Refer to Chapters "Ordering information" and "Functional description and testing".

SHORT TYPE NUMBER	DELIVERY FORMAT[1]	PERIOD t_T (s)	SPECIFICATIONS					
			PULSE WIDTH t_P (ms)	DRIVE (%)	DETECTION CRITERION	EEPROM	BATTERY EOL DETECTION	REMARKS
1485	U/7	1	5.8	75	P = 1 N = 2	yes	yes	
1486	U/7	1	5.8	75	P = 1 N = 2	yes	no	
1487	U/5	1	7.8	75	P = 2 N = 3	yes	yes	

Note

1. U = Chip in trays; U/5 = wafer; U/7 = chip with bumps on tape.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	V_{SS} = 0 V; note 1	−1.8	+6	V
V_I	all input voltages		V_{SS}	V_{DD}	V
	output short-circuit duration			indefinite	
T_{amb}	operating ambient temperature		−10	+60	°C
T_{stg}	storage temperature		−30	+100	°C

Note

1. Connecting the battery with reversed polarity does not destroy the circuit, but in this condition a large current flows, which will rapidly discharge the battery.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advisable to take handling precautions appropriate to handling MOS devices. Advice can be found in *"Data Handbook IC16, General, Handling MOS Devices"*.

CHARACTERISTICS

V_{DD} = 1.55 V; V_{SS} = 0 V; f_{osc} = 32.768 kHz; T_{amb} = 25 °C; crystal: R_S = 20 kΩ; C_1 = 2 to 3 fF; C_L = 8 to 10 pF; C_0 = 1 to 3 pF; unless otherwise specified.

Immunity against parasitic impedance = 20 MΩ from one pin to an adjacent pin.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD1}	supply voltage	T_{amb} = −10 to +60 °C	1.2	1.55	2.5	V
ΔV_{DD}	supply voltage variation	transient	–	–	0.25	V
V_{DD2}	supply voltage pulse	programming	5.0	5.1	5.2	V
ΔV_{DDP}	supply voltage pulse variation	programming	0.55	0.6	0.65	V
I_{DD1}	supply current	between motor pulses	–	170	260	nA
I_{DD2}	supply current	T_{amb} = −10 to +60 °C	–	–	600	nA
I_{DD3}	supply current	stop mode; pin 8 connected to V_{DD}	–	180	280	nA
Motor output						
V_{sat}	saturation voltage Σ (P + N)	R_M = 2 kΩ; T_{amb} = −10 to +60 °C	–	150	200	mV
$Z_{o(sc)}$	output short-circuit impedance	between motor pulses $I_{transistor}$ < 1 mA	–	200	300	Ω
Oscillator						
$V_{OSC\ ST}$	starting voltage		1.2	–	–	V
g_m	transconductance	$V_{i(p-p)} \leq$ 50 mV	6	15	–	µS
t_{osc}	start-up time		–	1	–	s
$\Delta f/f$	frequency stability	ΔV_{DD} = 100 mV	–	0.05×10^{-6}	0.3×10^{-6}	
C_i	input capacitance		8	10	12	pF
C_o	output capacitance		12	15	18	pF
Voltage level detector						
V_{EOL}	threshold voltage		1.30	1.38	1.46	V
ΔV_{EOL}	hysteresis of threshold		–	10	–	mV
TC_{EOL}	temperature coefficient		–	−1	–	mV/K
Reset input						
f_o	output frequency		–	32	–	Hz
ΔV_o	output voltage swing	R = 1 MΩ; C = 10 pF	1.4	–	–	V
t_{edge}	edge time	R = 1 MΩ; C = 10 pF	–	1	–	µs
I_{im}	peak input current	note 1	–	320	–	nA
$I_{i(av)}$	average input current		–	10	–	nA

Note

1. Duty factor is 1 : 32 and RESET = V_{DD} or V_{SS}.

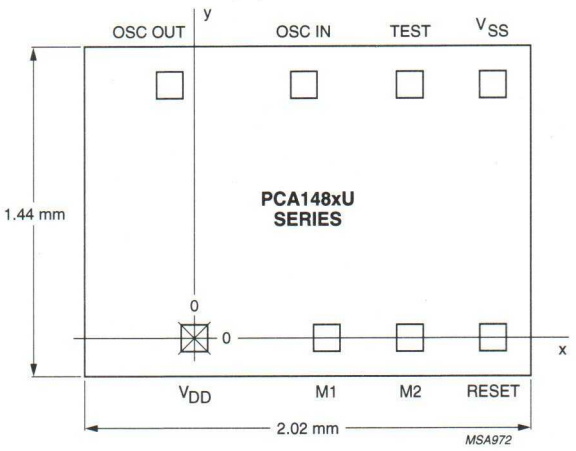
TIMING PARAMETERS

SYMBOL	PARAMETER	SECTION	VALUE	OPTION	UNIT
t_T	cycle for motor pulse (note 1)	motor pulse (Figs 2 and 3)	1	5, 10, 12 or 20	s
t_P	motor pulse width		7.81	3.9 or 5.9	ms
t_{DF}	duty factor		977	–	µs
t_{ONL}	last duty factor on		183 to 488	–	µs
t_v	voltage detection cycle	level mode	60	–	s
t_{SON}	duty factor on	silver-oxide mode (Fig.3)	427 to 733	–	µs
t_{SOFF}	duty factor off		550 to 244	–	µs
t_{SONF}	first duty factor on		244	–	µs
t_E	EOL sequence	end-of-life mode	4	–	s
t_{E1}	motor pulse width		t_P	–	ms
t_{E2}	time between pulses		31.25	–	ms
t_D	detection sequence	detection (Fig.6)	4.3 to 28.3	–	ms
t_{DS}	short-circuited motor		977	–	µs
t_{DI}	dissipation of energy		977	–	µs
t_{MC}	measurement cycle		488	–	µs
t_{M1}	phase 1		244	–	µs
t_{M2}	phase 2 (measure window)		61	–	µs
t_{M3}	phase 3		122	–	µs
t_{M4}	phase 4		61	–	µs
P	positive current polarities		2	P < N	
N	negative current polarities		3	2 to 6	
t_C	correction sequence	correction sequence (Fig.7)	t_P + 30.27	–	ms
t_{C1}	small pulse width		977	–	µs
t_{C2}	large pulse width		t_P	–	ms
	cycle time for motor pulses in:	testing			
t_{T1}	test 1		125	–	ms
t_{T2}	test 2		31.25	–	ms
t_{T3}	test 3	see Fig.9	31.25 to 39	–	ms
t_{DEB}	debounce time for RESET = V_{DD}		14.7 to 123.2	–	ms

Note

1. No option available when EOL indication is required.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



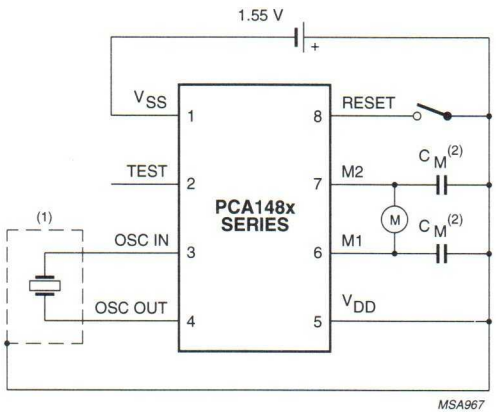
Chip area: 2.91 mm^2.
Bonding pad dimensions: 110 µm × 110 µm.
Chip thickness: 200 ±25 µm, with bumps: 270 ±25 µm.

Fig.10 Bonding pad locations, PCA148xU series; 8 terminals.

Table 3 Bonding pad locations (dimensions in µm)
All x/y coordinates are referenced to bottom left pad (V_{DD}), see Fig.10.

PAD	x	y
V_{SS}	1290	1100
TEST	940	1100
OSC IN	481	1100
OSC OUT	−102	1100
V_{DD}	0	0
M1	578	0
M2	930	0
RESET	1290	0
chip corner (max. value)	−497.5	−170

APPLICATION INFORMATION



(1) Quartz crystal case should be connected to V_{DD}. Stray capacitance and leakage resistance from RESET, M1 or M2 to OSC IN should be less than 0.5 pF or larger than 20 MΩ.

(2) Motor, probe and stray capacitance from M2 or M1 to V_{DD} or V_{SS} should be less than C_M = 80 pF for correct operation of the detection circuit. Driving the motor at its minimum energy, probe and stray capacitance must be avoided.

Fig.11 Typical application circuit diagram.

32 kHz watch circuits with EEPROM PCA16xx series

FEATURES

- 32 kHz oscillator, amplitude regulated with excellent frequency stability
- High immunity of the oscillator to leakage currents
- Time calibration electrically programmable and reprogrammable (via EEPROM)
- A quartz crystal is the only external component required
- Very low current consumption; typically 170 nA
- Detector for silver-oxide or lithium battery voltage levels
- Indication for battery end-of-life
- Stop function for accurate timing
- Power-on reset for fast testing
- Various test modes for testing the mechanical parts of the watch and the IC.

GENERAL DESCRIPTION

The PCA16xx series devices are CMOS integrated circuits specially suited for battery-operated, quartz-crystal-controlled wrist-watches, with bipolar stepping motors.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE[1]		
	NAME	DESCRIPTION	VERSION
PCA1601U/10	–	chip on foil	–
PCA1602T	PMFP8	plastic micro flat package; 8 leads (straight)	SOT144-1
PCA1603U/7	–	chip with bumps on tape	–
PCA1604U	–	chip in tray	–
PCA1604U/10	–	chip on foil	–
PCA1605U/7	–	chip with bumps on tape	–
PCA1606U/10	–	chip on foil	–
PCA1607U	–	chip in tray	–
PCA1608U	–	chip in tray	–
PCA1611U	–	chip in tray	–
PCA1621U/7	–	chip with bumps on tape	–
PCA1621U/10	–	chip on foil	–
PCA1622U	–	chip in tray	–
PCA1623U/7	–	chip with bumps on tape	–
PCA1624U	–	chip in tray	–
PCA1625U/7	–	chip with bumps on tape	–
PCA1626U	–	chip in tray	–
PCA1627U/7	–	chip with bumps on tape	–
PCA1628U	–	chip in tray	–
PCA1629U/7	–	chip with bumps on tape	–

Note

1. Figure 1 and Chapter "Package outline" show details of standard package, available for specified devices and for large orders only.
   Chapter "Chip dimensions and bonding pad locations" shows exact pad locations for other delivery formats.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{SS}	1	ground (0 V)
TEST	2	test output
OSC IN	3	oscillator input
OSC OUT	4	oscillator output
V_{DD}	5	positive supply voltage
M1	6	motor 1 output
M2	7	motor 2 output
RESET	8	reset input

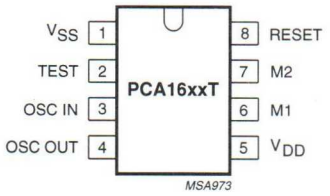


Fig.1 Pin configuration, PCA16xxT, (PMFP8).

FUNCTIONAL DESCRIPTION AND TESTING

Motor pulse

The motor pulse width (t_P) and the cycle times (t_T) are given in Chapter "Available types".

Voltage level detector

The supply voltage is compared with the internal voltage reference V_{LIT} and V_{EOL} every minute. The first voltage level detection is carried out 30 ms after a RESET.

Lithium mode

If a lithium voltage is detected ($V_{DD} \geq V_{LIT}$), the circuit will operate in the lithium mode. The motor pulse will be produced with a 75% duty factor.

Silver-oxide mode

If the voltage level detected is between V_{LIT} and V_{EOL}, the circuit will operate in silver-oxide mode.

Battery end-of-life[1]

If the battery end-of-life is detected ($V_{DD} \leq V_{EOL}$), the motor pulse will be produced without chopping. To indicate this condition, bursts of 4 pulses are produced every 4 s.

Power-on reset

For correct operation of the Power-on reset the rise time of V_{DD} from 0 V to 2.1 V should be less than 0.1 ms.
All resettable flip-flops are reset. Additionally the polarity of the first motor pulse is positive: $V_{M1} - V_{M2} \geq 0$ V.

Customer testing

An output frequency of 32 Hz is provided at RESET (pin 8) to be used for exact frequency measurement. Every minute a jitter occurs as a result of time calibration, which occurs 90 to 150 ms after disconnecting the RESET from V_{DD}.

Connecting the RESET to V_{DD} stops the motor pulses leaving them in a HIGH impedance 3-state condition and a 32 Hz signal without jitter is produced at the TEST pin. A debounce circuit protects accidental stoppages due to mechanical shock to the watch (t_{DEB} = 14.7 to 123.2 ms).

Connecting RESET to V_{SS} activates Tests 1 and 2 and disables the time calibration.

Test 1, $V_{DD} > V_{EOL}$. Normal function takes place except the voltage detection cycle (t_V) is 125 ms and the cycle time t_{T1} is 31.25 ms. At pin TEST a minute signal is available at 8192 times its normal frequency.

Test 2[2], $V_{DD} < V_{EOL}$. The voltage detection cycle (t_V) is 31.25 ms and the motor pulse period (t_{T2}) = 31.25 ms.

Test and reset mode are terminated by disconnecting the RESET pin.

Test 3, $V_{DD} > 5.1$ V. Motor pulses with a time period of t_{T3} = 31.25 ms and n × 122 µs are produced to check the contents of the EEPROM. At pin TEST the motor pulse period signal (t_T) is available at 1024 times its normal frequency. The circuit returns to normal operation when $V_{DD} < 2.5$ V between two motor pulses.

(1) Only available for types with a 1 s motor pulse.

(2) Only applicable for types with the battery end-of-life detector.

Time calibration

Taking a normal quartz crystal with frequency 32768kHz, frequency deviation ($\Delta f/f$) of $\pm 15 \times 10^{-6}$ and C_L = 8.2 pF; the oscillator frequency is offset (by using non-symmetrical internal oscillator input and output capacitances of 10 pF and 15 pF) such that the frequency deviation is positive-only. This positive deviation can then be compensated for to maintain time-keeping accuracy.

Once the positive frequency deviation is measured, a corresponding number 'n' (see Table 1) is programmed into the device's EEPROM. This causes n pulses of frequency 8192 Hz to be inhibited every minute of operation, which achieves the required calibration.

The programming circuit is shown in Fig.2. The required number n is programmed into EEPROM by varying V_{DD} according to the steps shown in Fig.3, which are explained below:

1. The positive quartz frequency deviation ($\Delta f/f$) is measured, and the corresponding values of n are found according to Table 1.
2. V_{DD} is increased to 5.1 V allowing the contents of the EEPROM to be checked from the motor pulse period t_{T3} at nominal frequency.
3. V_{DD} is decreased to 2.5 V during a motor pulse to initialize a storing sequence.
4. The first V_{DD} pulse to 5.1 V erases the contents of EEPROM.
5. When the EEPROM is erased a logic 1 is at the TEST pin.
6. V_{DD} is increased to 5.1 V to read the data by pulsing V_{DD} n times to 4.5 V. After the n edge, V_{DD} is decreased to 2.5 V.
7. V_{DD} is increased to 5.1 V to store n bits in the EEPROM.
8. V_{DD} is decreased to 2.5 V to terminate the storing sequence and to return to operating mode.
9. V_{DD} is increased to 5.1 V to check writing from the motor pulse period t_{T3}.
10. V_{DD} is decreased to the operation voltage **between** two motor pulses to return to operating mode. (Decreasing V_{DD} during the motor pulse would restart the programming mode).

The time calibration can be reprogrammed up to 100 times.

Table 1 Quartz crystal frequency deviation, n and t_{T3}

FREQUENCY DEVIATION $\Delta f/f$ ($\times 10^{-6}$)	NUMBER OF PULSES (n)	t_{T3} (ms)
0[1]	0	31.250[2]
+2.03	1	31.372
+4.06	2	31.494
.	.	.
.	.	.
.	.	.
+127.89	63	38.936

Notes

1. Increments of 2.03×10^{-6}/step.
2. Increments of 122 µs/step.

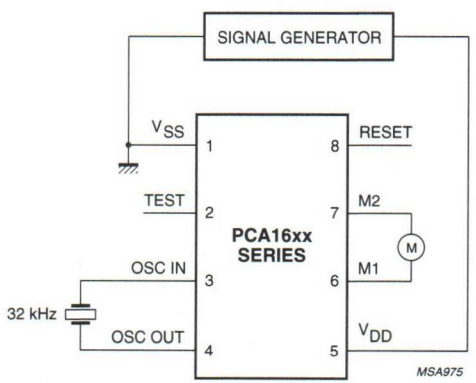
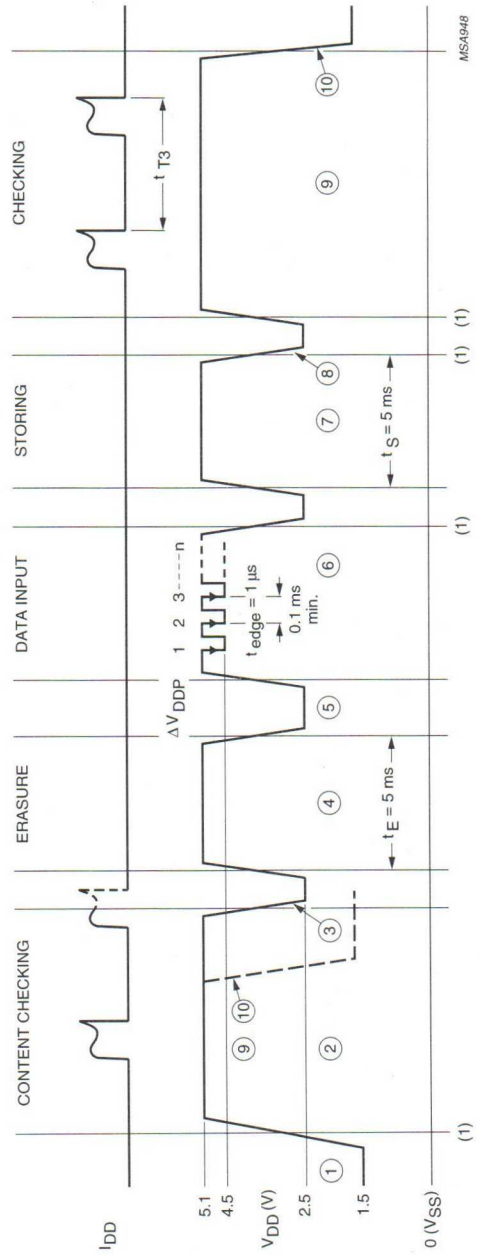


Fig.2 Circuit for programming the time calibration.



(1) Rise and fall time should be greater than 400 µs/V for immediately correct checking.

Fig.3 V_{DD} for programming.

AVAILABLE TYPES

Refer to Fig.4 and to Chapters "Ordering information" and "Functional description and testing".

SHORT TYPE NUMBER	DELIVERY FORMAT[1]	PERIOD t_T (s)	SPECIFICATIONS				
			PULSE WIDTH t_P (ms)	DRIVE (%)	EEPROM	BATTERY EOL DETECTION	REMARKS
1601	U/10	1	7.8	100	yes	no	
1602	T	1	7.8	75	yes	no	
1603	U/7	20	7.8	100	yes	no	
1604	U/10	5	7.8	75	yes	no	
1605	U/7	5	4.8	75	yes	no	
1606	U/10	10	6.8	100	yes	no	
1607	U	5	5.8	100 75	yes	no	1.5 V and 2.1 V Lithium
1608	U	5	7.8	100 75	yes	no	1.5 V and 2.1 V Lithium
1611	U	1	6.8	75	yes	no	
1621	U/7	20	4.8	100	yes	no	
1622	U	1	4.8	100	yes	yes	
1623	U	20	4.8	75	yes	no	
1624	U	12	3.9	75 56	yes	no	1.5 V and 2.1 V Lithium
1625	U/7	5	5.8	75	yes	no	
1626	U	20	5.8	100	yes	no	
1627	U/7	20	5.8	100 75	yes	no	1.5 V and 2.1 V Lithium
1628	U	20	5.8	75	yes	no	
1629	U/7	5	6.8	75	yes	no	

Note

1. U = Chip in trays; U/7 = chip with bumps on tape; U/10 = chip on foil.
   T = SOT144-1.

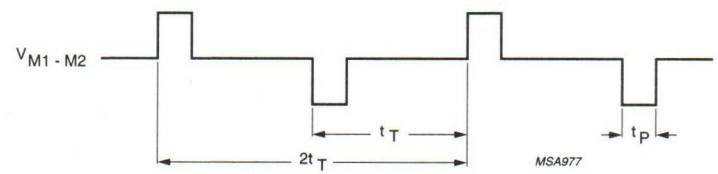


Fig.4 Motor output waveform (normal operation).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	V_{SS} = 0 V; note 1	−1.8	+6	V
V_I	all input voltages		V_{SS}	V_{DD}	V
	output short-circuit duration			indefinite	
T_{amb}	operating ambient temperature		−10	+60	°C
T_{stg}	storage temperature		−30	+100	°C

Note

1. Connecting the battery with reversed polarity does not destroy the circuit, but in this condition a large current flows, which will rapidly discharge the battery.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advisable to take handling precautions appropriate to handling MOS devices. Advice can be found in *"Data Handbook IC16, General, Handling MOS Devices"*.

CHARACTERISTICS

V_{DD} = 1.55 V; V_{SS} = 0 V; f_{osc} = 32.768 kHz; T_{amb} = 25 °C; crystal: R_S = 20 kΩ; C_1 = 2 to 3 fF; C_L = 8 to 10 pF; C_0 = 1 to 3 pF; unless otherwise specified.

Immunity against parasitic impedance = 20 MΩ from one pin to an adjacent pin.

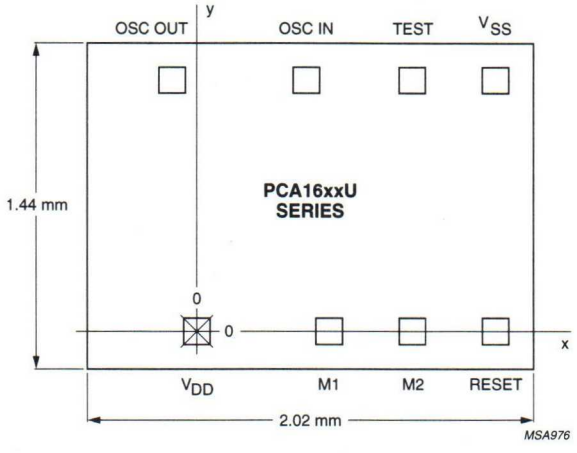
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	T_{amb} = −10 to +60 °C	1.2	1.5	2.5	V
ΔV_{DD}	supply voltage variation	transient; V_{DD} = 1.2 to 2.5 V	–	–	0.25	V
V_{DDP}	supply voltage pulse	programming	5.0	5.1	5.2	V
ΔV_{DDP}	supply voltage pulse variation	programming	0.55	0.6	0.65	V
I_{DD1}	supply current	between motor pulses	–	170	260	nA
I_{DD2}	supply current	between motor pulses; V_{DD} = 2.1 V	–	190	300	nA
I_{DD3}	supply current	stop mode; pin 8 connected to V_{DD}	–	180	280	nA
I_{DD4}	supply current	stop mode; pin 8 connected to V_{DD}; V_{DD} = 2.1 V	–	220	360	nA
I_{DD5}	supply current	V_{DD} = 2.1 V; T_{amb} = −10 to +60 °C	–	–	600	nA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Motor output						
V_{sat}	saturation voltage Σ (P + N)	R_L = 2 kΩ; T_{amb} = −10 to +60 °C	–	150	200	mV
R_{sc}	short-circuit resistance Σ (P + N)	$I_{transistor}$ < 1 mA	–	200	300	Ω
t_T	cycle time		note 1			
t_P	pulse width		note 2			
Oscillator						
$V_{OSC\ ST}$	starting voltage		1.2	–	–	V
g_m	transconductance	$V_{i(p-p)} \leq 50$ mV	6	15	–	µS
t_{osc}	start-up time		–	1	–	s
Δf/f	frequency stability	ΔV_{DD} = 100 mV	–	0.05×10^{-6}	0.3×10^{-6}	
C_i	input capacitance		8	10	12	pF
C_o	output capacitance		12	15	18	pF
Voltage level detector						
V_{LIT}	threshold voltage	lithium mode	1.65	1.80	1.95	V
V_{EOL}	threshold voltage	battery end-of-life	1.27	1.38	1.46	V
ΔV_{VLD}	hysteresis of threshold		–	10	–	mV
TC_{VLD}	temperature coefficient		–	−1	–	mV/K
t_V	voltage detection cycle		–	60	–	s
Reset input						
f_o	output frequency		–	32	–	Hz
ΔV_o	output voltage swing	R = 1 MΩ; C = 10 pF	1.4	–	–	V
t_{edge}	edge time	R = 1 MΩ; C = 10 pF	–	1	–	µs
I_{im}	peak input current	note 3	–	320	–	nA
$I_{i(av)}$	average input current		–	10	–	nA
Test mode						
	cycle time for motor pulses in:					
t_{T1}	test 1		–	125	–	ms
t_{T2}	test 2		–	31.25	–	ms
t_{T3}	test 3		see Chapter "Available types"			
t_{DEB}	debounce time	RESET = V_{DD}	14.7	–	123.2	ms
Battery end-of-life						
t_{EOL}	end-of-life sequence		–	4	–	s
t_{E1}	motor pulse width	see "Available types"	–	t_P	–	ms
t_{E2}	time between pulses		–	31.25	–	ms

Notes

1. Cycle time can be changed to one of the following values: 1, 5, 10, 12 or 20 s (see Chapter "Available types").
2. Pulse width can be varied from 2 ms to 15.7 ms in steps of 1 ms (see Chapter "Available types").
3. Duty factor is 1 : 32 and RESET = V_{DD} or V_{SS}.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



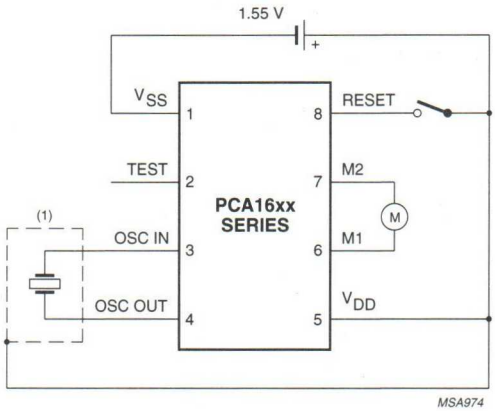
Chip area: 2.91 mm^2.
Bonding pad dimensions: 110 µm × 110 µm.
Chip thickness: 200 ±25 µm, with bumps: 270 ±25 µm.

Fig.5 Bonding pad locations, PCA16xxU series, 8 terminals.

Table 2 Bonding pad locations (dimensions in µm)
All x/y coordinates are referenced to the centre of pad (V_{DD}), see Fig.5.

PAD	x	y
V_{SS}	1290	1100
TEST	940	1100
OSC IN	481	1100
OSC OUT	−102	1100
V_{DD}	0	0
M1	578	0
M2	930	0
RESET	1290	0
chip corner (max. value)	−497.5	−170

APPLICATION INFORMATION



(1) Quartz crystal case should be connected to V_{DD}. Stray capacitance and leakage resistance from RESET, M1 or M2 to OSC IN should be less than 0.5 pF or larger than 20 MΩ.

Fig.6 Typical application circuit diagram.

32 kHz watch circuits using a silver-oxide or a 3 V lithium battery

PCA167x series

FEATURES

- 32 kHz oscillator, amplitude regulated with excellent frequency stability
- High immunity of the oscillator to leakage currents
- Very low current consumption; typically 150 nA
- Stop function for accurate timing
- Chopped motor pulses available
- Power-on reset for fast testing
- Various test modes for testing the mechanical parts of the watch and the IC.

GENERAL DESCRIPTION

The PCA167x series devices are CMOS integrated circuits specially suited for battery-operated, quartz-crystal-controlled wrist-watches, with a bipolar stepping motor.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE[1]		
	NAME	DESCRIPTION	VERSION
PCA1672U	–	chip in tray	–
PCA1673U	–	chip in tray	–
PCA1675U	–	chip in tray	–
PCA1676U/10	–	chip on foil	–
PCA1677U	–	chip in tray	–

Note

1. Figure 1 and Chapter "Package outline" show details of standard package, available for large orders only. Chapter "Chip dimensions and bonding pad locations" shows exact pad locations for other delivery formats.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{SS}	1	ground (0 V)
TEST	2	test output
OSC IN	3	oscillator input
OSC OUT	4	oscillator output
V_{DD}	5	positive supply voltage
M1	6	motor 1 output
M2	7	motor 2 output
RESET	8	reset input

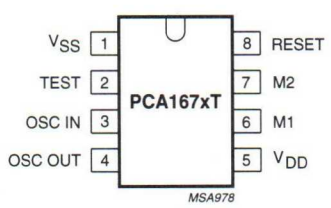


Fig.1 Pin configuration, PCA167xT, (PMFP8).

FUNCTIONAL DESCRIPTION AND TESTING

Motor pulse

The motor output pulse widths (t_P) and the cycle times (t_T) are given in Chapter "Available types".

Power-on reset

For correct operation of the Power-on reset the rise time of V_{DD} from 0 V to 1.55 V should be less than 0.1 ms.
All resettable flip-flops are reset. Additionally the polarity of the first motor pulse is positive: $V_{M1} - V_{M2} \geq 0$ V.

Customer testing and stop mode

An output frequency of 32 Hz is provided at RESET (pin 8) to be used for exact frequency measurement.

Connecting the RESET to V_{DD} stops the motor pulses leaving them in a HIGH impedance 3-state condition and a 32 Hz signal is produced at the TEST pin. A debounce circuit protects against accidental stoppages due to mechanical shock to the watch (t_{DEB} = 14.7 to 123.2 ms).

Connecting RESET to V_{SS} activates the test mode.
The motor pulse period is 31.25 ms instead of t_T. Test and stop mode are disabled by disconnecting RESET (open-circuit).

AVAILABLE TYPES

Refer to Fig.2 and to Chapters "Ordering information" and "Functional description and testing".

SHORT TYPE NUMBER	DELIVERY FORMAT(1)	PERIOD t_T (s)	SPECIFICATIONS				
			PULSE WIDTH t_P (ms)	DRIVE (%)	EEPROM	BATTERY EOL DETECTION	REMARKS
1672	U	1	7.8	56	no	no	3 V Lithium
1673	U	1	5.8	56	no	no	3 V Lithium
1675	U	1/16	5.8	100	no	no	no oscillator
1676	U/10	10	5.8	56	no	no	3 V Lithium
1677	U	10	7.8	100	no	no	1.5 V

Note

1. U = Chip in trays; U/10 = chip on foil.

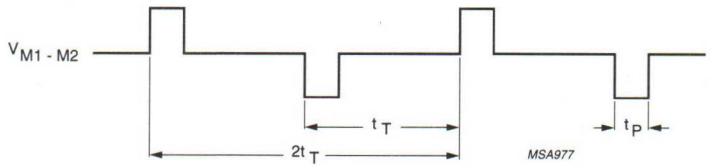


Fig.2 Motor output waveform (normal operation).

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	V_{SS} = 0 V; note 1	−1.8	+6	V
V_I	all input voltages		V_{SS}	V_{DD}	V
	output short-circuit duration		indefinite		
T_{amb}	operating ambient temperature		−10	+60	°C
T_{stg}	storage temperature		−30	+100	°C

Note

1. Connecting the battery with reversed polarity does not destroy the circuit, but in this condition a large current flows, which will rapidly discharge the battery.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advisable to take handling precautions appropriate to handling MOS devices. Advice can be found in *"Data Handbook IC16, General, Handling MOS Devices"*.

CHARACTERISTICS

V_{DD} = 1.55 V; V_{SS} = 0 V; f_{osc} = 32.768 kHz; T_{amb} = 25 °C; crystal: R_S = 20 kΩ; C_1 = 2 to 3 fF; C_L = 8 to 10 pF; C_0 = 1 to 3 pF; unless otherwise specified.

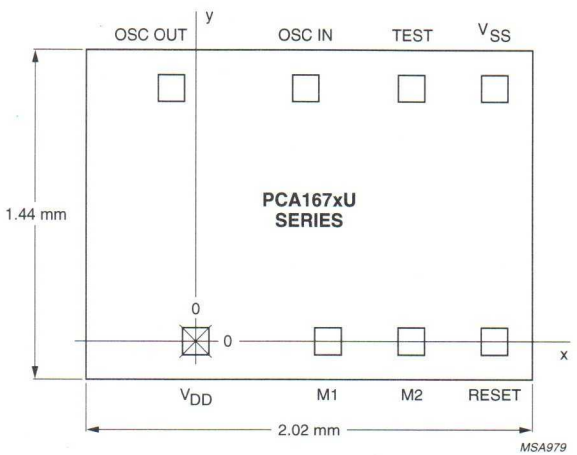
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	T_{amb} = −10 to +60 °C	1.2	1.5	3.5	V
ΔV_{DD}	supply voltage variation	transient; V_{DD} = 1.2 to 3.5 V	–	–	0.25	V
I_{DD1}	supply current	between motor pulses	–	150	250	nA
I_{DD2}	supply current	between motor pulses; V_{DD} = 3.5 V	–	200	350	nA
I_{DD3}	supply current	stop mode; pin 8 connected to V_{DD}	–	180	300	nA
I_{DD4}	supply current	stop mode; pin 8 connected to V_{DD}; V_{DD} = 3.5 V	–	300	480	nA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Motor output						
V_{sat}	saturation voltage Σ (P + N)	R_L = 2 kΩ; T_{amb} = −10 to +60 °C	–	150	200	mV
R_{sc}	short-circuit resistance Σ (P + N)	$I_{transistor}$ < 1 mA	–	200	300	Ω
t_T	cycle time		note 1			
t_P	pulse width		note 2			
Oscillator						
$V_{OSC\ ST}$	starting voltage		1.2	–	–	V
g_m	transconductance	$V_{i(p-p)}$ = 50 mV	6	15	–	µS
t_{osc}	start-up time		–	1	–	s
Δf/f	frequency stability	ΔV_{DD} = 100 mV	–	0.05×10^{-6}	0.3×10^{-6}	
C_i	input capacitance		–	3	–	pF
C_o	output capacitance		19	24	29	pF
Reset input						
f_o	output frequency		–	32	–	Hz
ΔV_o	output voltage swing	R = 1 MΩ; C = 10 pF	1.4	–	–	V
t_{edge}	edge time	R = 1 MΩ; C = 10 pF	–	1	–	µs
I_{im}	peak input current	note 3	–	320	–	nA
$I_{i(av)}$	average input current		–	10	–	nA
Test mode						
t_{T1}	cycle time		–	31.25	–	ms
t_{DEB}	debounce time	RESET = V_{DD}	14.7	–	123.2	ms

Notes

1. Cycle time can be changed to one of the following values: 1, 5, 10, 12 or 20 s (see Chapter "Available types").
2. Pulse width can be varied from 2 ms to 15.7 ms in steps of 1 ms (see Chapter "Available types").
3. Duty factor is 1 : 32 and RESET = V_{DD} or V_{SS}.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



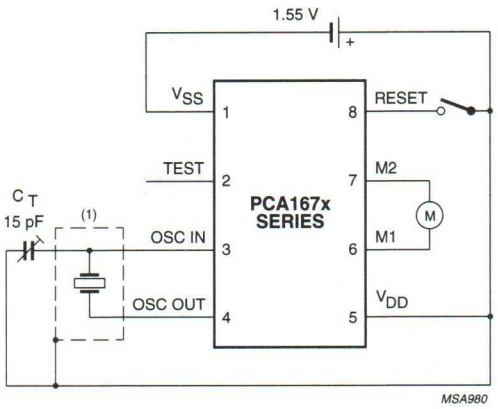
Chip area: 2.91 mm^2.
Bonding pad dimensions: 110 µm × 110 µm.
Chip thickness: 200 ±25 µm, with bumps: 270 ±25 µm.

Fig.3 Bonding pad locations, PCA167xU series; 8 terminals.

Table 1 Bonding pad locations (dimensions in µm)
All x/y coordinates are referenced to the centre of pad (V_{DD}), see Fig.3.

PAD	x	y
V_{SS}	1290	1100
TEST	940	1100
OSC IN	481	1100
OSC OUT	−102	1100
V_{DD}	0	0
M1	578	0
M2	930	0
RESET	1290	0
chip corner (max. value)	−497.5	−170

APPLICATION INFORMATION



(1) Quartz crystal case should be connected to V_{DD}. Stray capacitance and leakage resistance from RESET, M1 or M2 to OSC IN should be less than 0.5 pF or larger than 20 MΩ.

Fig.4 Typical application circuit diagram.

4-digit LCD car clock PCF1171C

FEATURES

- Driving standard 3½ or a 4-digit LCD
- Internal voltage regulator for 5 V LCD
- Option for external stabilized voltage supply
- 4.19 MHz oscillator
- Integrated oscillator output capacitor and polarization resistor
- Operating ambient temperature: −40 to +85 °C
- 40-lead plastic SMD, face down (VSO40).

GENERAL DESCRIPTION

The PCF1171C is a single chip, 4.19 MHz CMOS car clock circuit indicating hours and minutes. It is designed to drive a 3½ or 4-digit liquid crystal display (LCD).

Two external single-pole, single-throw switches will accomplish all time setting functions. A bonding option allows the selection of 12-hour or 24-hour display mode. The circuit is battery-operated via an internal 5 V voltage regulator or by an external stabilized voltage supply.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF1171CT	VSO40	plastic very small outline package; 40 leads; face down[1]	SOT158-2
PCF1171CU	–	uncased chip in tray[2]	–

Notes

1. See Fig.1 and Chapter "Package outline" for pin layout and package details.
2. See Chapter "Chip dimensions and bonding pad locations" for pad layout and package details.

PINNING

SYMBOL	PIN	DESCRIPTION
OSC OUT	1	oscillator output
OSC IN	2	oscillator input
S1	3	set hour
S3	4	±2 minute correction
BP	5	64 Hz backplane driver (common of LCD)
ADEG1	6	segment driver
C1	7	segment driver
E2	8	segment driver
D2	9	segment driver
C2	10	segment driver
E3	11	segment driver
D3	12	segment driver
C3	13	segment driver
E4	14	segment driver
D4	15	segment driver
C4	16	segment driver
B4	17	segment driver
S2	18	set minutes
S4	19	internal voltage regulation
V_{SS}	20	negative supply
S6	21	selectable correction mode
S5	22	12/24-hour mode
V_{DD}	23	positive supply
A4	24	segment driver
F4	25	segment driver
G4	26	segment driver
B3	27	segment driver
A3	28	segment driver
F3	29	segment driver
G3	30	segment driver
P1, P2	31	colon flashing
P3, P4	32	colon static
B2	33	segment driver
A2	34	segment driver
F2	35	segment driver
G2	36	segment driver
B1	37	segment driver
TR	38	test reset; connect to (V_{DD})
TS	39	test speed-up; connect to (V_{DD})
(V_{DD})	40	positive supply for test and oscillator inputs

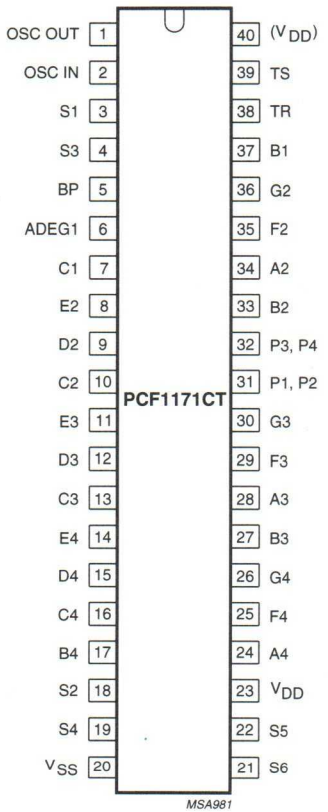


Fig.1 Pin configuration, PCF1171CT, (VSO40).

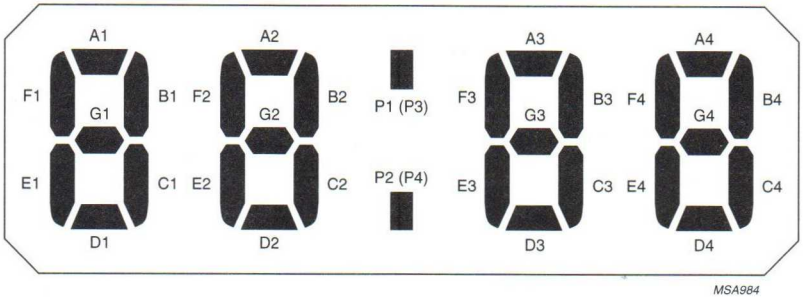


Fig.2 Segment designation of LCD.

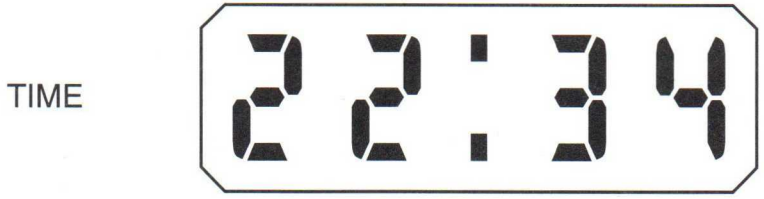


Fig.3 Display mode (24-hour mode shown).

OPERATIONAL INPUTS

Operational inputs S1, S2 and S3 have an internal pull-up resistor to facilitate use of external single-pole, single-throw switches. A specific debounce circuit is integrated as protection against contact debounce and parasitic voltages.

In the description below, an arrangement as shown in Fig.5 is assumed and S1, S2 and S3 refer to the external switches rather than the corresponding inputs.

Set hours, switch S1

Closure of S1 increments the hours according to the correction mode selected by S6 (see Chapter "Input options").

Set minutes/reset seconds, switch S2

When S2 is closed, the minute setting is corrected according to the correction mode determined by S6 (see Chapter "Input options").

The seconds counter is reset to zero each time S2 is closed, and begins running each time S2 is opened.

Segment test/reset, switches S1 and S2

If S1 and S2 are closed simultaneously all LCD segments are switched on. When the switches are released, the clock starts at 1 : 00 in the 12-hour mode or 0 : 00 in the 24-hour mode.

Time correction ±2 minutes, switch S3

This switch operates in two ranges:

- Displayed time ≥ 58 minutes 00 seconds
- Displayed time ≤ 1 minute 59 seconds.

When switch S3 is pressed in these ranges, the minutes and seconds are reset to zero. For displayed time ≥ 58 minutes 00 seconds, the hour is also incremented by one.

INPUT OPTIONS

In the description below S4, S5 and S6 refer to the external switches shown in Fig.5 rather than to the corresponding inputs.

In a real application, these inputs will normally be bonded to the appropriate level to give the required function mode.

Internal/external regulation, switch S4

For internal regulation, S4 is closed, the internal voltage regulator is active and the voltage supply for the LCD is regulated to 5 V. For external regulation, S4 is open and the circuit has to be supplied with an externally regulated voltage.

12/24-hour mode, switch S5

For 12-hour display mode, S5 is connected to V_{DD}.
For 24-hour display mode, S5 is connected to V_{SS}.

Single/continuous correction mode, switch S6

For single-set correction mode, S6 is connected to V_{DD}. Each closure of S1 or S2 advances the counter by one.

For continuous-set correction mode, S6 is connected to V_{SS}. Momentary closure of S1 or S2 causes single increments as for single-set correction mode. If S1 or S2 is kept closed for more than 1s, the counter is automatically incremented by 1 for each full second that S1 or S2 is kept closed.

TESTING

In normal operation the test inputs TR (pin 38) and TS (pin 39) have to be connected to V_{DD} (pin 23). A test frequency (64 Hz) is available at BP (pin 5). The test mode is activated by connecting TS to V_{SS} (pin 20). All output frequencies are then increased by a factor of 65536. In this mode the maximum input frequency is 100 kHz (external generator at OSC IN). By connecting TR to V_{SS} all counters (seconds, minutes and hours) are stopped. After connecting TR to V_{DD} all counters start from an initial state.

The switches/inputs described above also operate in the test mode.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage with respect to V_{SS} with internal regulation disconnected;	note 1	–	8	V
V_I	all input voltages		V_{SS} – 0.3	V_{DD} + 0.3	V
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–55	+125	°C

Note

1. Connecting the supply voltage with reverse polarity, will not harm the circuit, provided the current is limited to 10 mA by the external resistor.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advisable to take handling precautions appropriate to handling MOS devices. Advice can be found in *"Data Handbook IC16, General, Handling MOS Devices"*.

CHARACTERISTICS

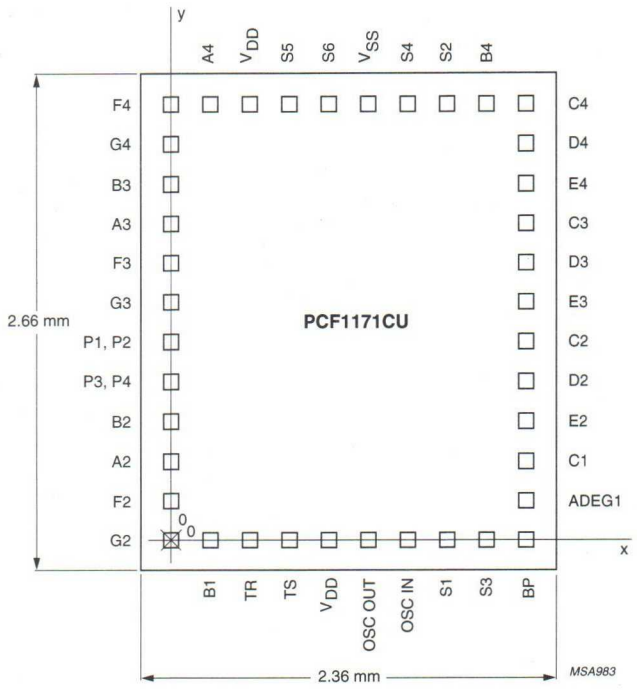
V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; crystal: f = 4.194304 MHz; R_s = 50 Ω; C_L = 12 pF; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage					
	external regulation		3	–	6	V
	internal regulation	I_{REG} = 1 mA	4	5	6	V
I_{REG}	regulation current with internal regulation		0.2	–	5	mA
I_{DD}	current consumption	all switches open; without LCD; internal regulation disconnected; note 1	50	400	700	µA
r_o	differential internal impedance	I_{REG} = 1 mA	–	–	150	Ω
Oscillator (pins 1 and 2) (see note 2)						
t_{osc}	start time		–	–	200	ms
$\Delta f/f_{osc}$	frequency stability	ΔV_{DD} = 100 mV	–	0.2×10^{-6}	1×10^{-6}	
R_{fb}	feedback resistance		0.1	–	1	MΩ
C_i	input capacitance		–	–	9	pF
C_o	output capacitance		19	24	29	pF
Switches S1, S2 and S3 (pins 18, 3 and 4) and test inputs, TS, TR (pins 38 and 39)						
I_i	input current	with inputs connected to V_{SS}	50	150	500	µA
t_d	debounce time		32	–	150	ms
R_S	segment driver output resistance	I_L = ±50 µA	–	1	2.5	kΩ
R_{BP}	backplane driver output resistance	I_L = ±250 µA	–	0.2	0.5	kΩ
f_{BP}	backplane driver output frequency		–	64	–	Hz
$V_{offset(DC)}$	LCD DC offset voltage	R_L = 200 kΩ; C_L = 1 nF	–	–	±50	mV

Notes

1. The current $I_{EXT} = I_{REG} + I_{DD} + 2 \times I_i$ (+ LCD current).
2. For correct operation of the oscillator: $V_{DD} \geq 3$ V.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 6.28 mm^2.
Bonding pad dimensions: 110 μm × 110 μm.
Chip thickness: 381 ±25 μm.

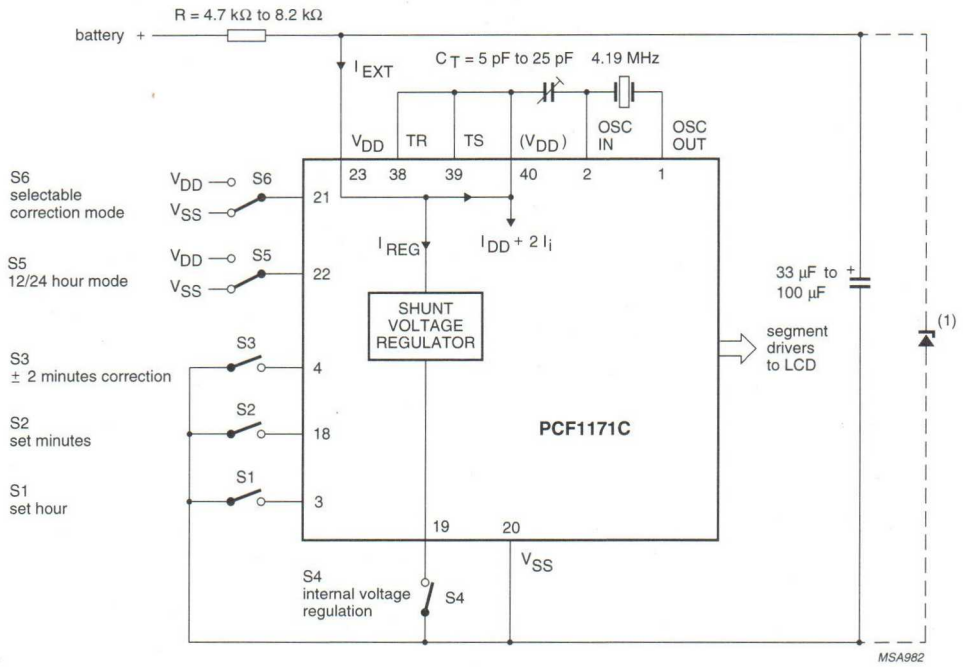
Fig.4 Bonding pad locations, PCF1171CU; 40 terminals.

Table 1 Bonding pad locations (dimensions in μm)

All x/y coordinates are referenced to the pad G2, see Fig.4.

PAD	x	y	PAD	x	y
OSC OUT	1060	0	S6	860	2320
OSC IN	1260	0	S5	660	2320
S1	1460	0	V_{DD}	460	2320
S3	1680	0	A4	240	2320
BP	1920	0	F4	0	2320
ADEG1	1920	240	G4	0	2080
C1	1920	460	B3	0	1860
E2	1920	660	A3	0	1660
D2	1920	860	F3	0	1460
C2	1920	1060	G3	0	1260
E3	1920	1260	P1, P2	0	1060
D3	1920	1460	P3, P4	0	860
C3	1920	1660	B2	0	660
E4	1920	1860	A2	0	460
D4	1920	2080	F2	0	240
C4	1920	2320	G2	0	0
B4	1680	2320	B1	240	0
S2	1460	2320	TR	460	0
S4	1260	2320	TS	660	0
V_{SS}	1060	2320	V_{DD}	860	0
chip corner (max. value)	−220	−170			

APPLICATION INFORMATION



(1) Only required if internal regulation is disconnected.

From pin 2 (OSC IN) to any other pin the stray capacitance should not exceed 2 pF.

Fig.5 Typical application diagram.

$3^1/_2$-digit LCD car clock PCF1172C

FEATURES

- Driving standard $3^1/_2$-digit LCD with AM and PM indicators
- Internal voltage regulator for 5 V LCD
- Option for external stabilized voltage supply
- 4.19 MHz oscillator
- Integrated oscillator output capacitor and polarization resistor
- Operating ambient temperature: –40 to +85 °C
- 40-lead plastic SMD, face down (VSO40).

GENERAL DESCRIPTION

The PCF1172C is a single chip, 4.19 MHz CMOS clock circuit indicating hours and minutes. It is designed to drive a $3^1/_2$-digit liquid crystal display (LCD) with AM and PM indicators.

Two external single-pole, single-throw switches will accomplish all time setting functions. The circuit is battery-operated via an internal 5 V voltage regulator or by an external stabilized voltage supply.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF1172CT	VSO40	plastic very small outline package; 40 leads; face down[1]	SOT158-2
PCF1172CU	–	uncased chip in tray[2]	–

Notes

1. See Fig.1 and Chapter "Package outline" for pin layout and package details.
2. See Chapter "Chip dimensions and bonding pad locations" for pad layout and package details.

PINNING

SYMBOL	PIN	DESCRIPTION
OSC OUT	1	oscillator output
OSC IN	2	oscillator input
S1	3	set hour
S3	4	±2 minute correction
BP	5	64 Hz backplane driver (common of LCD)
PM	6	segment output for PM annunciator
AM	7	segment output for AM annunciator
E2	8	segment driver
D2	9	segment driver
C2	10	segment driver
E3	11	segment driver
D3	12	segment driver
C3	13	segment driver
E4	14	segment driver
D4	15	segment driver
C4	16	segment driver
B4	17	segment driver
S2	18	set minutes
S4	19	internal voltage regulation
V_{SS}	20	negative supply
S6	21	selectable correction mode
n.c.	22	not connected
V_{DD}	23	positive supply
A4	24	segment driver
F4	25	segment driver
G4	26	segment driver
B3	27	segment driver
A3	28	segment driver
F3	29	segment driver
G3	30	segment driver
P1, P2	31	colon flashing
P3, P4	32	colon static
B2	33	segment driver
A2	34	segment driver
F2	35	segment driver
G2	36	segment driver
B1, C1	37	segment driver
TR	38	test reset; connect to (V_{DD})
TS	39	test speed-up; connect to (V_{DD})
(V_{DD})	40	positive supply for test and oscillator inputs

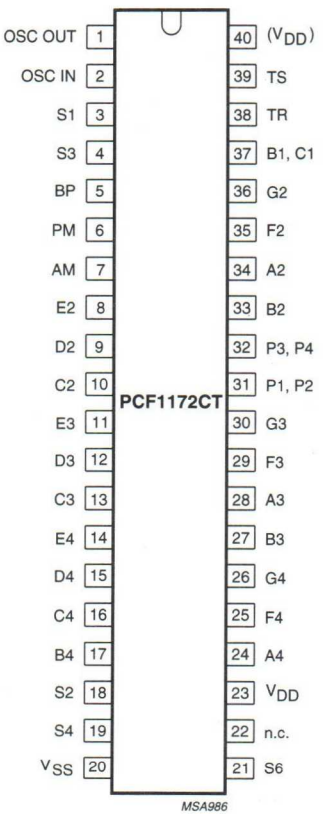


Fig.1 Pin configuration, PCF1172CT, (VSO40).

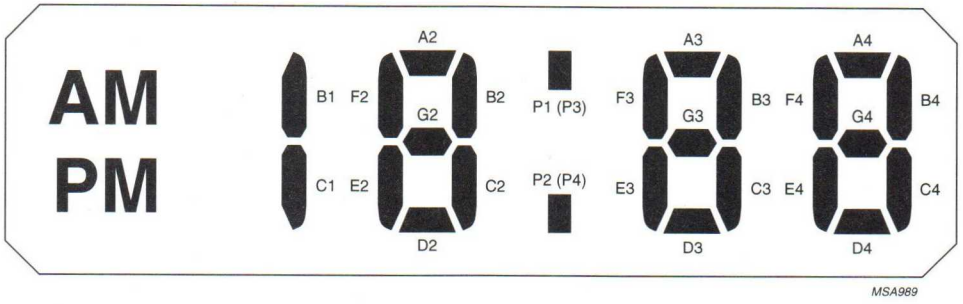


Fig.2 Segment designation of LCD.

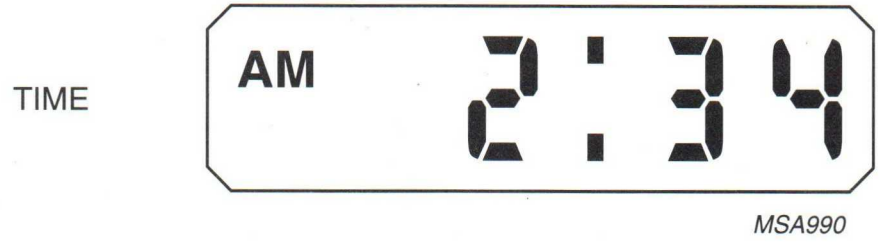


Fig.3 Display mode (12-hour with AM/PM annunciator).

OPERATIONAL INPUTS

Operational inputs S1, S2 and S3 have an internal pull-up resistor to facilitate use of external single-pole, single-throw switches. A specific debounce circuit is integrated as protection against contact debounce and parasitic voltages.

In the description below, an arrangement as shown in Fig.5 is assumed and S1, S2 and S3 refer to the external switches rather than the corresponding inputs.

Set hours, switch S1

Closure of S1 increments the hours according to the correction mode selected by S6 (see Chapter "Input options").

Set minutes/reset seconds, switch S2

When S2 is closed, the minute setting is corrected according to the correction mode determined by S6 (see Chapter "Input options").

The seconds counter is reset to zero each time S2 is closed, and begins running each time S2 is opened.

Segment test/reset, switches S1 and S2

If S1 and S2 are closed simultaneously all LCD segments are switched on. When the switches are released, the clock starts at 1 : 00.

Time correction ±2 minutes, switch S3

.This switch operates in two ranges:

- Displayed time ≥ 58 minutes 00 seconds
- Displayed time ≤ 1 minute 59 seconds.

When switch S3 is pressed in these ranges, the minutes and seconds are reset to zero. For displayed time ≥ 58 minutes 00 seconds, the hour is also incremented by one.

INPUT OPTIONS

In the description below S4 and S6 refer to the external switches shown in Fig.5 rather than to the corresponding inputs.

In a real application, these inputs will normally be bonded to the appropriate level to give the required function mode.

Internal/external regulation, switch S4

For internal regulation, S4 is closed, the internal voltage regulator is active and the voltage supply for the LCD is regulated to 5 V. For external regulation, S4 is open and the circuit has to be supplied with an externally regulated voltage.

Single/continuous correction mode, switch S6

For single-set correction mode, S6 is connected to V_{DD}. Each closure of S1 or S2 advances the counter by one.

For continuous-set correction mode, S6 is connected to V_{SS}. Momentary closure of S1 or S2 causes single increments as for single-set correction mode. If S1 or S2 is kept closed for more than 1s, the counter is automatically incremented by 1 for each full second that S1 or S2 is kept closed.

TESTING

In normal operation the test inputs TR (pin 38) and TS (pin 39) have to be connected to V_{DD} (pin 23). A test frequency (64 Hz) is available at BP (pin 5). The test mode is activated by connecting TS to V_{SS} (pin 20). All output frequencies are then increased by a factor of 65536. In this mode the maximum input frequency is 100 kHz (external generator at OSC IN). By connecting TR to V_{SS} all counters (seconds, minutes and hours) are stopped. After connecting TR to V_{DD} all counters start from an initial state.

The switches/inputs described above also operate in the test mode.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage with respect to V_{SS} with internal regulation disconnected	note 1	–	8	V
V_I	all input voltages		V_{SS} – 0.3	V_{DD} + 0.3	V
T_{amb}	operating ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–55	+125	°C

Note

1. Connecting the supply voltage with reverse polarity, will not harm the circuit, provided the current is limited to 10 mA by the external resistor.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advisable to take handling precautions appropriate to handling MOS devices. Advice can be found in *"Data Handbook IC16, General, Handling MOS Devices"*.

CHARACTERISTICS

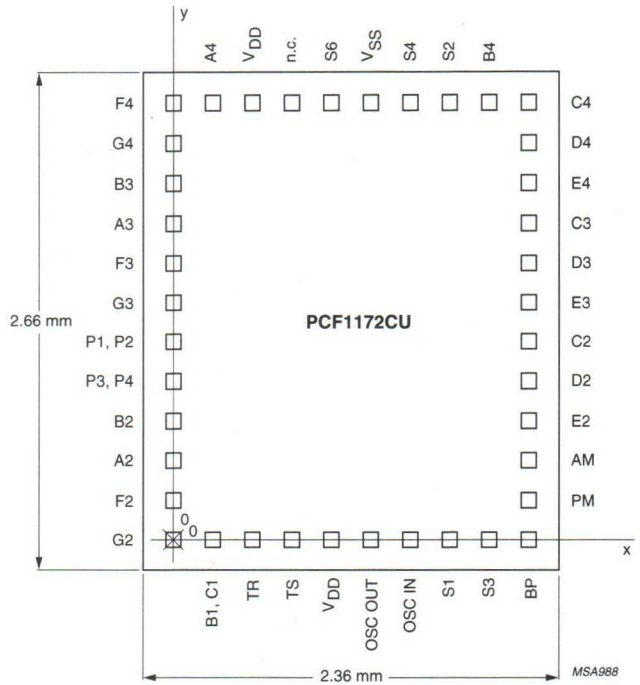
V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; crystal: f = 4.194304 MHz; R_s = 50 Ω; C_L = 12 pF; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	external regulation	3	–	6	V
	external regulation		3	–	6	V
	internal regulation	I_{REG} = 1 mA	4	5	6	V
I_{REG}	regulation current with internal regulation		0.2	–	5	mA
I_{DD}	current consumption	all switches open; without LCD; internal regulation disconnected; note 1	50	400	700	µA
r_o	differential internal impedance	I_{REG} = 1 mA	–	–	150	Ω
Oscillator (pins 1 and 2; note 2)						
t_{osc}	start time		–	–	200	ms
$\Delta f/f_{osc}$	frequency stability	ΔV_{DD} = 100 mV	–	0.2×10^{-6}	1×10^{-6}	
R_{fb}	feedback resistance		0.1	–	1	MΩ
C_i	input capacitance		–	–	9	pF
C_o	output capacitance		19	24	29	pF
Switches S1, S2 and S3 (pins 18, 3 and 4)						
I_i	input current	with inputs connected to V_{SS}	50	150	500	µA
t_d	debounce time		32	–	150	ms
R_S	segment driver output resistance	I_L = ±50 µA	–	1	2.5	kΩ
R_{BP}	backplane driver output resistance	I_L = ±250 µA	–	0.2	0.5	kΩ
f_{BP}	backplane driver output frequency		–	64	–	Hz
$V_{offset(DC)}$	LCD DC offset voltage	R_L = 200 kΩ; C_L = 1 nF	–	–	±50	mV

Notes

1. The current $I_{EXT} = I_{REG} + I_{DD} + 2 \times I_i$ (+ LCD current).
2. For correct operation of the oscillator: $V_{DD} \geq 3$ V.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



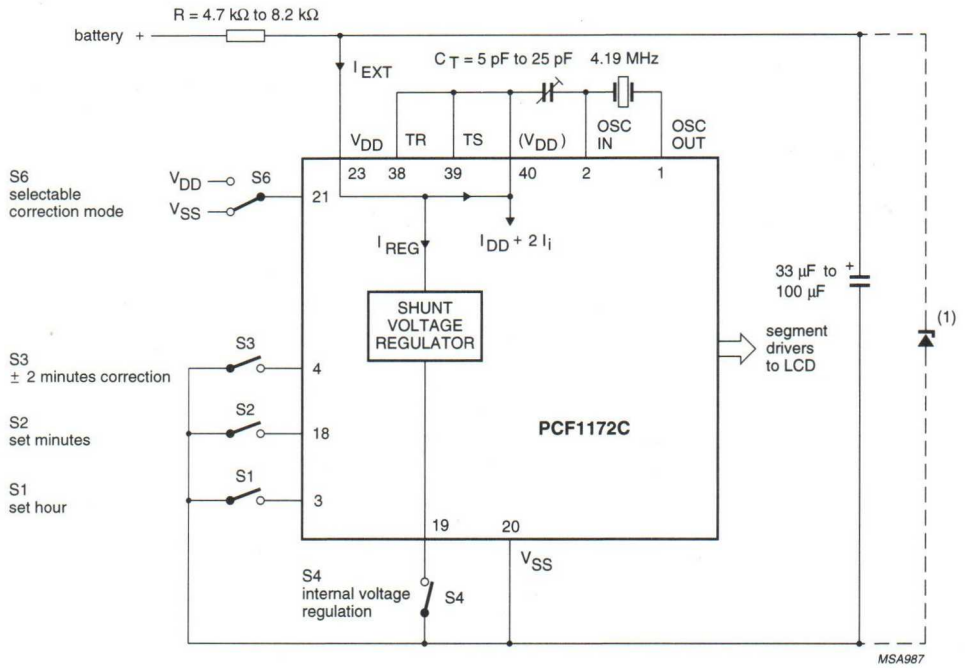
n.c. = not connected.
Chip area: 6.28 mm^2.
Bonding pad dimensions: 110 µm × 110 µm.
Chip thickness: 381 ±25 µm.

Fig.4 Bonding pad locations, PCF1172CU; 40 terminals.

Table 1 Bonding pad locations (dimensions in μm)
All x/y coordinates are referenced to the pad G2, see Fig.4.

PAD	x	y	PAD	x	y
OSC OUT	1060	0	S6	860	2320
OSC IN	1260	0	n.c.	660	2320
S1	1460	0	V_{DD}	460	2320
S3	1680	0	A4	240	2320
BP	1920	0	F4	0	2320
PM	1920	240	G4	0	2080
AM	1920	460	B3	0	1860
E2	1920	660	A3	0	1660
D2	1920	860	F3	0	1460
C2	1920	1060	G3	0	1260
E3	1920	1260	P1, P2	0	1060
D3	1920	1460	P3, P4	0	860
C3	1920	1660	B2	0	660
E4	1920	1860	A2	0	460
D4	1920	2080	F2	0	240
C4	1920	2320	G2	0	0
B4	1680	2320	B1, C1	240	0
S2	1460	2320	TR	460	0
S4	1260	2320	TS	660	0
V_{SS}	1060	2320	V_{DD}	860	0
chip corner (max. value)	−220	−170			

APPLICATION INFORMATION



(1) Only required if internal regulation is disconnected.
From pin 2 (OSC IN) to any other pin the stray capacitance should not exceed 2 pF.

Fig.5 Typical application diagram.

4-digit static LCD car clock PCF1174C

FEATURES

- Internal voltage regulator is electrically programmable for various LCD voltages
- Time calibration is electrically programmable (no trimming capacitor required)
- LCD voltage adjusts with temperature for good contrast
- 4.19 MHz oscillator
- 12-hour or 24-hour mode
- Operating ambient temperature: –40 to +85 °C
- 40-lead plastic SMD, face down (VSO40).

GENERAL DESCRIPTION

The PCF1174C is a single chip, 4.19 MHz CMOS car clock circuit providing hours, minutes and seconds functions. It is designed to drive a 4-digit static liquid crystal display (LCD).

Two external single-pole, single-throw switches will accomplish all time setting functions. Time calibration and voltage regulator are electrically programmable via an on-chip EEPROM. The circuit is battery-operated via an internal voltage regulator and an external resistor.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF1174CT	VSO40	plastic very small outline package; 40 leads; face down[1]	SOT158-2
PCF1174CU	–	uncased chip in tray[2]	–

Notes

1. See Fig.1 and Chapter "Package outline" for pin layout and package details.
2. See Chapter "Chip dimensions and bonding pad locations" for pad layout and package details.

PINNING

SYMBOL	PIN	DESCRIPTION
BP	1	backplane output
PM	2	segment driver
AM	3	segment driver
ADEG1	4	segment driver
C1	5	segment driver
E2	6	segment driver
D2	7	segment driver
C2	8	segment driver
E3	9	segment driver
C3	10	segment driver
E4	11	segment driver
D4	12	segment driver
C4	13	segment driver
B4	14	segment driver
S1	15	hour adjustment input
DATA	16	EEPROM data input
OSC IN	17	oscillator input
OSC OUT	18	oscillator output
V_{SS}	19	negative supply
MODE	20	12/24-hour mode select input
V_{PP}	21	programming voltage input
TS	22	test speed-up mode input
ENABLE	23	set enable input for S1 and S2
V_{DD}	24	positive supply voltage
FLASH	25	colon option input
SEL	26	EEPROM select input
S2	27	minute adjustment input
A4	28	segment driver
F4	29	segment driver
G4	30	segment driver
B3	31	segment driver
AD3	32	segment driver
F3	33	segment driver
G3	34	segment driver
COL	35	segment driver
B2	36	segment driver
A2	37	segment driver
F2	38	segment driver
G2	39	segment driver
B1	40	segment driver

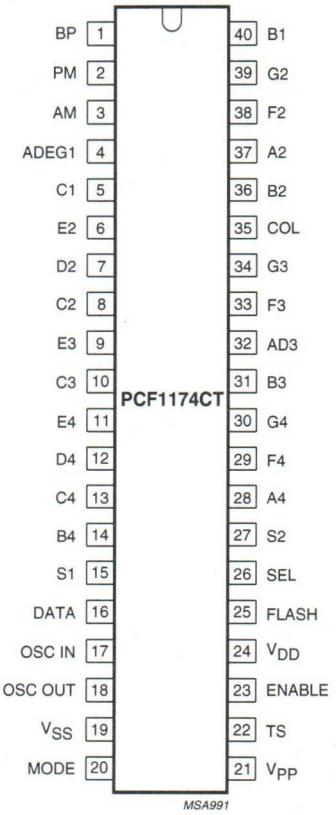


Fig.1 Pin configuration, PCF1174CT, (VSO40).

FUNCTIONAL DESCRIPTION AND TESTING

Outputs

The circuit outputs static data to the LCD. Generation of BP and the output signals are shown in Fig.4.

The average voltages across the segments are:

1. $V_{ON(RMS)} = V_{DD}$
2. $V_{OFF(RMS)} = 0$ V.

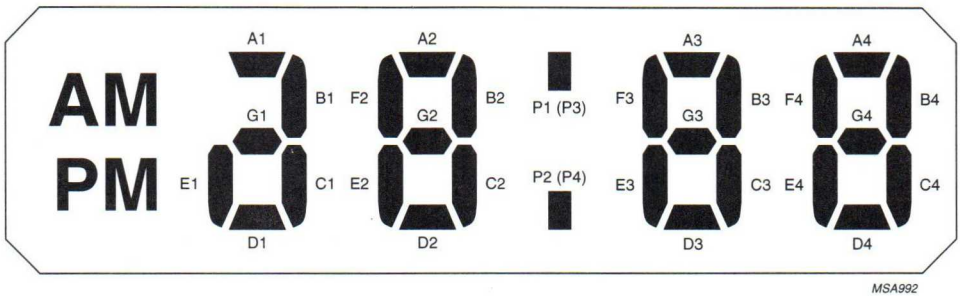
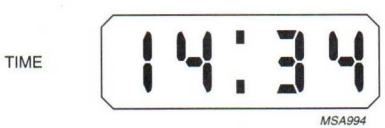


Fig.2 Segment designation of LCD.



(a)

a. 12-hour mode.



(b)

b. 24-hour mode.

Fig.3 Typical displays.

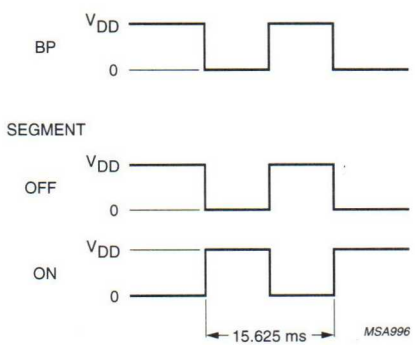


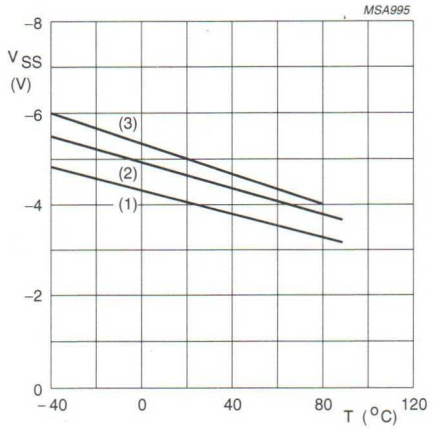
Fig.4 Backplane and output signals.

LCD voltage (see Fig.5)

The adjustable voltage regulator controls the supply voltage (see Section "LCD voltage programming") in relation to temperature for good contrast, for example when V_{DD} = 4.5 V at +25 °C, then:

V_{DD} = 3 to 4 V at +85 °C.

V_{DD} = 5 to 6 V at −40 °C.



(1) Programmed to 4.0 V at 25 °C (value within the specified operating range).
(2) Programmed to 4.5 V at 25 °C (value within the specified operating range).
(3) Programmed to 5.0 V at 25 °C (value within the specified operating range).

Fig.5 Regulated voltage as a function of temperature (typical).

12/24-hour mode

Operation in 12-hour or 24-hour mode is selected by connecting MODE to V_{DD} or V_{SS} respectively.

Power-on

After connecting the supply, the start-up mode is:

1:00 AM; 12-hour mode.

0:00; 24-hour mode.

Colon

If FLASH is connected to V_{DD} the colon pulses at 1 Hz. If FLASH is connected to V_{SS} the colon is static.

Time setting

Switch inputs S1 and S2 have a pull-up resistor to facilitate the use of single-pole, single-throw contacts. A debounce circuit is incorporated to protect against contact bounce and parasitic voltages.

Set enable

Inputs S1 and S2 are enabled by connecting ENABLE to V_{DD} or disabled by connecting to V_{SS}.

Set hours

When S1 is connected to V_{SS} the hours displayed advances by one and after one second continues with one advance per second until S1 is released (auto-increment).

Set minutes

When S2 is connected to V_{SS} the time displayed in minutes advances by one and after one second continues with one advance per second until S2 is released (auto-increment). In addition to minute correction, the seconds counter is reset to zero.

Segment test/reset

When S1 and S2 are connected to V_{SS}, all LCD segments are switched ON. Releasing switches S1 and S2 resets the display. No reset occurs when DATA is connected to V_{SS} (overlapping S1 and S2).

Test mode

When TS is connected to V_{DD}, the device is in normal operating mode. When connecting TS to V_{SS} all counters (seconds, minutes and hours) are stopped, allowing quick testing of the display via S1 and S2 (debounce and auto-increment times are 64 times faster). TS has a pull-up resistor but for reasons of safety it should be connected to V_{DD}.

EEPROM

V_{PP} has a pull-up resistor but for reasons of safety it should be connected to V_{DD}.

LCD voltage programming

To enable LCD voltage programming, SEL is set to open-circuit and a level of $V_{DD} - 5$ V is applied to V_{PP} (see Fig.6). The first pulse (t_E) applied to the DATA input clears the EEPROM to give the lowest voltage output. Further pulses (t_L) will increment the output voltage by steps of typically 150 mV (T_{amb} = 25 °C).
For programming, measure $V_{DD} - V_{SS}$ and apply a store pulse (t_W) when the required value is reached. If the maximum number of steps (n = 31) is reached and an additional pulse is applied the voltage will return to the lowest value.

Time calibration

To compensate for the tolerance in the quartz crystal frequency which has been positively offset (nominal deviation $+60 \times 10^{-6}$) by capacitors at the oscillator input and output, a number (n) of 262144 Hz pulses are inhibited every second of operation.

The number (n) is stored in a non-volatile memory which is achieved by the following steps (see Fig.6):

1. Set SEL to V_{SS} and a level of $V_{DD} - 5$ V to V_{PP}
2. The quartz-frequency deviation $\Delta f/f$ is measured and (n) is calculated (see Table 1)
3. A first pulse t_E is applied to the DATA input clears the EEPROM to give the highest backplane frequency
4. The calculated pulses (n) are entered in (t_H, t_L). If the maximum backplane period is reached and an additional pulse is applied the period will return to the lowest value.
5. The backplane period is controlled and (when correct) fixed by applying the store pulse t_W
6. Release SEL and V_{PP}.

Table 1 Time calibration ($\Delta t = 3.81$ µs; SEL at V_{SS})

OSCILLATOR-FREQUENCY DEVIATION $\Delta f/f$ ($\times 10^{-6}$)	NUMBER OF PULSES (n)	BACKPLANE PERIOD (ms)
0	0	15.625
+3.8	1	15.629
+7.6	2	15.633
+11.4	3	15.636
.	.	.
.	.	.
.	.	.
+117.8	31	15.743

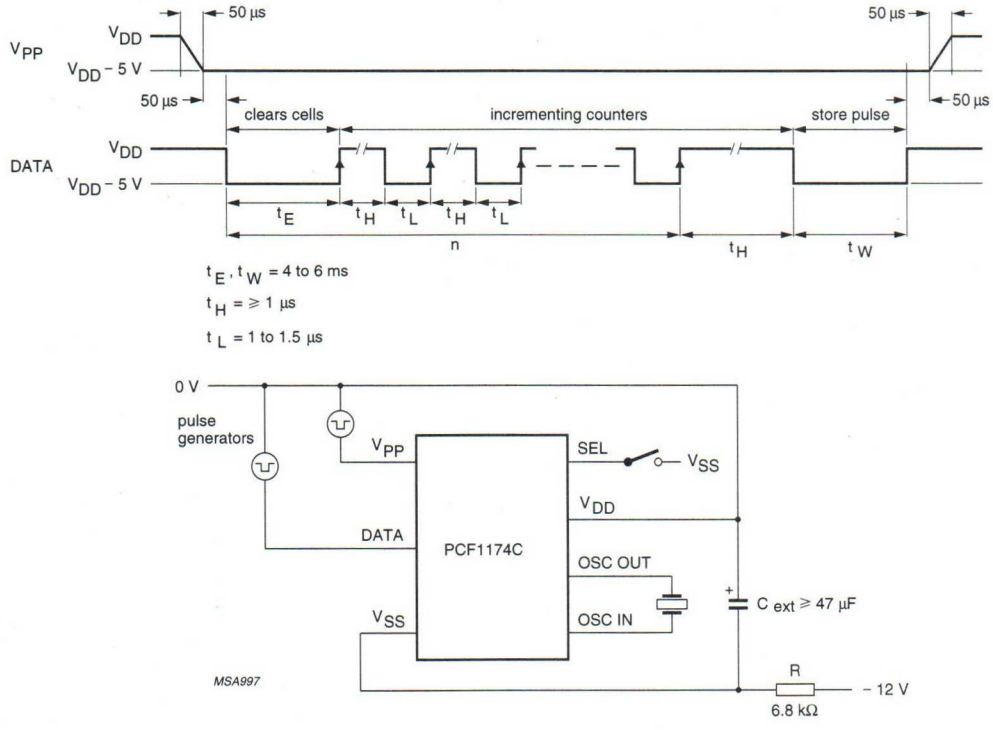


Fig.6 Programming diagram.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	with respect to V_{SS}	–	8	V
I_{DD}	supply current	V_{SS} = 0 V; note 1	–	3	mA
V_I	input voltage	all pins except V_{PP} and DATA	−0.3	V_{DD} + 0.3	V
		pins V_{PP} and DATA	−3	V_{DD} + 0.3	V
T_{amb}	operating ambient temperature		−40	+85	°C
T_{stg}	storage temperature		−55	+125	°C

Note

1. Connecting the supply voltage with reverse polarity, will not harm the circuit, provided the current is limited to 10 mA by the external resistor.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advisable to take handling precautions appropriate to handling MOS devices. Advice can be found in *"Data Handbook IC16, General, Handling MOS Devices"*.

CHARACTERISTICS

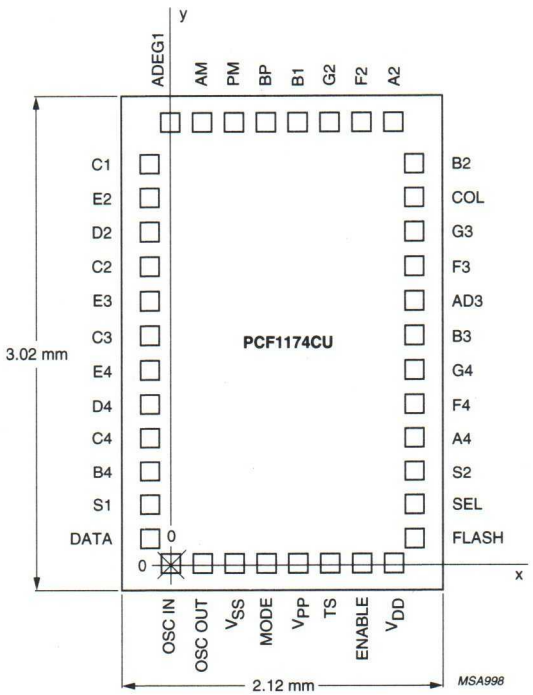
V_{DD} = 3 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; crystal: f = 4.194304 MHz; R_s = 50 Ω; C_L = 12 pF; maximum frequency tolerance = $\pm 30 \times 10^{-6}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	voltage regulator programmed to 4.5 V at T_{amb} = 25 °C	3	–	6	V
ΔV_{DD}	supply voltage variation	S1 or S2 closed	–	–	50	mV
TC	supply voltage variation due to temperature		–	−0.35	–	%/K
		V_{DD} = 4.5 V	–	−16	–	mV/K
I_{DD}	supply current	note 1	700	950	–	µA
C_{EXT}	capacitance	external capacitor	47	–	–	µF
Oscillator						
t_{osc}	start time		–	–	200	ms
Δf/f	frequency deviation	nominal n = 0	0	60×10^{-6}	110×10^{-6}	
Δf/f	frequency stability	ΔV_{DD} = 100 mV	–	–	1×10^{-6}	
R_{fb}	feedback resistance		300	1000	3000	kΩ
C_i	input capacitance		–	16	–	pF
C_o	output capacitance		–	27	–	pF
Inputs						
R_O	pull-up resistance	S1, S2, TS, SEL and DATA	45	90	180	kΩ
I_{IL}	leakage current	FLASH, ENABLE, MODE	–	–	2	µA
t_d	debounce time	S1 and S2 only	30	65	100	ms
V_{PP} programming voltage						
I_{O2}	output current	$V_{PP} = V_{DD} - 5$ V	70	–	700	µA
		during programming	–	500	–	µA
Backplane (high and low levels)						
R_{BP}	output resistance	±100 µA	–	–	3	kΩ
Segment						
R_{SEG}	output resistance	±100 µA	–	–	5	kΩ
LCD						
$V_{offset(DC)}$	DC offset voltage	200 kΩ/1 nF	–	–	50	mV

Note

1. A suitable resistor (R) must be selected (example):
   a) V_{DD} = 5 V; R max. (12 V − 5 V)/700 µA = 10 kΩ.
   b) V_{DD} = 5 V; R typ. (12 V − 5 V)/900 µA = 7.8 kΩ (more reserve).
   c) I_{DD} must not exceed 3 mA.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 6.4 mm^2.
Bonding pad dimensions: 110 µm × 110 µm.
Chip thickness: 381 ±25 mm.

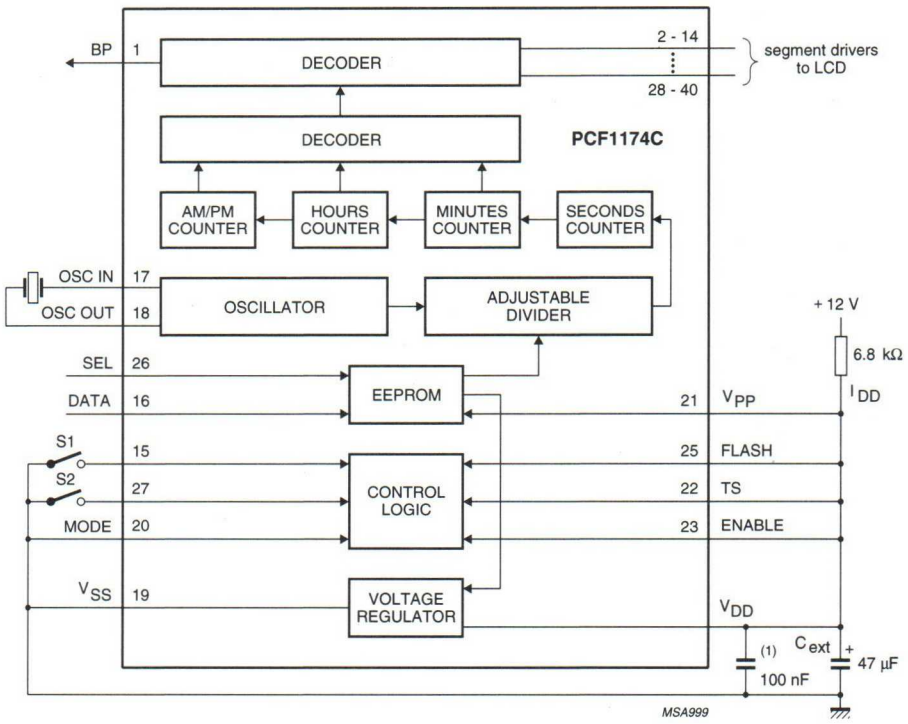
Fig.7 Bonding pad locations, PCF1174CU; 40 terminals.

Table 2 Bonding pad locations (dimensions in μm)

All x/y coordinates are referenced to the bottom left pad (OSC IN), see Fig.7.

PAD	x	y	PAD	x	y
BP	600	2676	V_{PP}	800	0
PM	400	2676	TS	1000	0
AM	200	2676	ENABLE	1200	0
ADEG1	0	2676	V_{DD}	1400	0
C1	−138	2448	FLASH	1538	168
E2	−138	2228	SEL	1538	388
D2	−138	2008	S2	1538	608
C2	−138	1808	A4	1538	808
E3	−138	1608	F4	1538	1008
C3	−138	1408	G4	1538	1208
E4	−138	1208	B3	1538	1408
D4	−138	1008	AD3	1538	1608
C4	−138	808	F3	1538	1808
B4	−138	608	G3	1538	2008
S1	−138	388	COL	1538	2208
DATA	−138	168	B2	1538	2448
OSC IN	0	0	A2	1400	2676
OSC OUT	200	0	F2	1200	2676
V_{SS}	400	0	G2	1000	2676
MODE	600	0	B1	800	2676
chip corner (max. value)	−360	−170			

APPLICATION INFORMATION



(1) To be placed close to the IC.

Fig.8 Typical application diagram.

4-digit duplex LCD car clock PCF1175C

FEATURES

- Internal voltage regulator is electrically programmable for various LCD voltages
- Time calibration is electrically programmable (no trimming capacitor required)
- LCD voltage adjusts with temperature for good contrast
- 4.19 MHz oscillator
- 12-hour or 24-hour mode
- Operating ambient temperature: –40 to +85 °C
- 28-lead plastic SMD (SO28)
- 1 Hz set mode.

GENERAL DESCRIPTION

The PCF1175C is a single chip, 4.19 MHz CMOS car clock circuit providing hours, minutes and seconds functions. It is designed to drive a 4-digit duplex liquid crystal display (LCD).

Two external single-pole, single-throw switches will accomplish all time setting functions. Time calibration and voltage regulator are electrically programmable via an on-chip EEPROM. The circuit is battery-operated via an internal voltage regulator and an external resistor.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF1175CT	SO28	plastic small outline package; 28 leads; body width 7.5 mm[1]	SOT136-1
PCF1175CU	–	uncased chip in tray[2]	–
PCF1175CU/10	–	chip-on-film frame carrier (FFC)[2]	–

Notes

1. See Fig.1 and Chapter "Package outline" for pin layout and package details.
2. See Chapter "Chip dimensions and bonding pad locations" for pad layout and package details.

PINNING

SYMBOL	PIN	DESCRIPTION
S1	1	hour adjustment input
DATA	2	EEPROM data input
OSC IN	3	oscillator input
OSC OUT	4	oscillator output
V_{SS}	5	negative supply voltage
MODE	6	12/24-hour mode select input
V_{PP}	7	programming voltage input
TS	8	test speed-up mode input
ENABLE	9	enable input (for S1 and S2)
V_{DD}	10	positive supply voltage
FLASH	11	colon option input
SEL	12	EEPROM select input
S2	13	minute adjustment input
B4/C4	14	segment driver
G4/D4	15	segment driver
F4/E4	16	segment driver
B3/C3	17	segment driver
G3/AD3	18	segment driver
F3/E3	19	segment driver
A4/COL	20	segment driver
B2/C2	21	segment driver
G2/D2	22	segment driver
F2/E2	23	segment driver
B1/C1	24	segment driver
A2/ADEG1	25	segment driver
AM/PM	26	segment driver
BP2	27	backplane 2
BP1	28	backplane 1

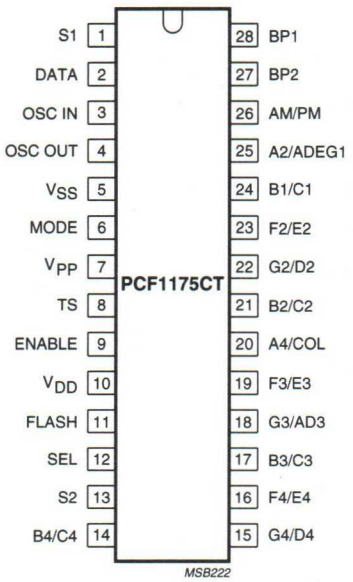


Fig.1 Pin configuration, PCF1175CT, (SO28).

FUNCTIONAL DESCRIPTION AND TESTING

Outputs

The circuit outputs 1 : 2 multiplexed data (duplex) to the LCD. Generation of BP1 and BP2 (three-level backplane signals) and the output signals are shown in Fig.4.

The average voltages across the segments are:

1. $V_{ON(RMS)} = 0.79\ V_{DD}$
2. $V_{OFF(RMS)} = 0.35\ V_{DD}$.

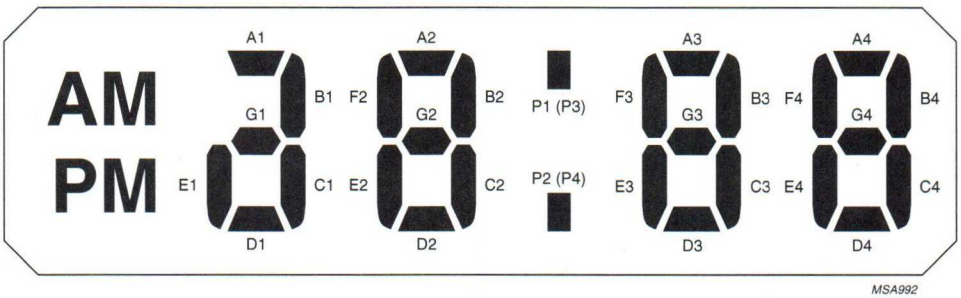
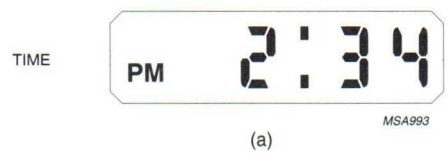
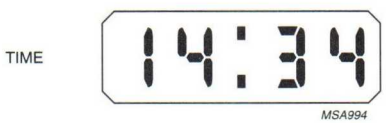


Fig.2 Segment designation of LCD.



(a)

a. 12-hour mode.



(b)

b. 24-hour mode.

Fig.3 Typical displays.

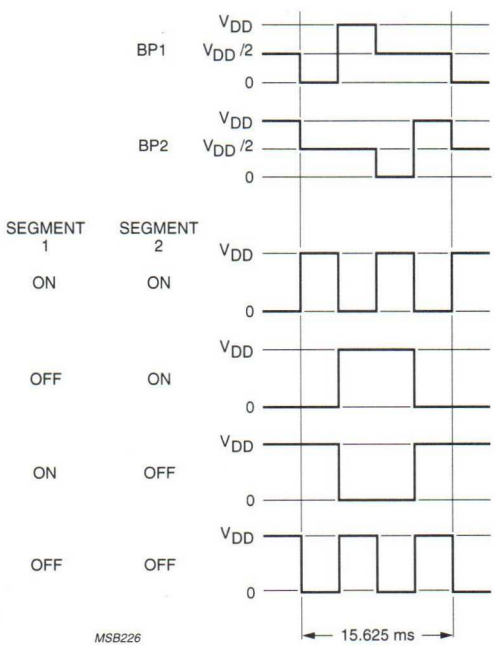


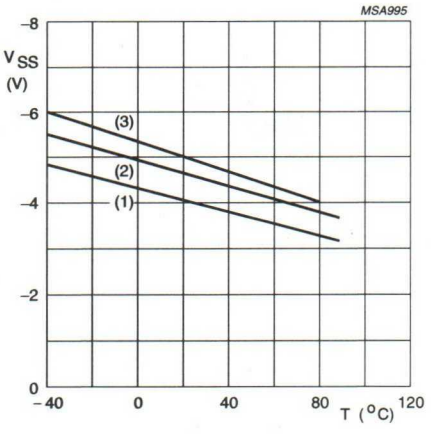
Fig.4 Backplane and output signals.

LCD voltage (see Fig.5)

The adjustable voltage regulator controls the supply voltage (see Section "LCD voltage programming") in relation to temperature for good contrast, for example when V_{DD} = 4.5 V at +25 °C, then:

V_{DD} = 3 to 4 V at +85 °C.

V_{DD} = 5 to 6 V at –40 °C.



(1) Programmed to 4.0 V at 25 °C (value within the specified operating range).
(2) Programmed to 4.5 V at 25 °C (value within the specified operating range).
(3) Programmed to 5.0 V at 25 °C (value within the specified operating range).

Fig.5 Regulated voltage as a function of temperature (typical).

12/24-hour mode

Operation in 12-hour or 24-hour mode is selected by connecting MODE to V_{DD} or V_{SS} respectively. If MODE is left open-circuit and a reset occurs, the mode will change from 12-hour to 24-hour mode or vice versa.

Power-on

After connecting the supply, the start-up mode is:

MODE connected to V_{DD}: 12-hour mode, 1:00 AM.

MODE connected to V_{SS}: 12-hour mode, 0:00.

MODE left open-circuit: 24-hour mode, 0:00 or 1:00.

Colon

If FLASH is connected to V_{DD} the colon pulses at 1 Hz. If FLASH is connected to V_{SS} the colon is static.

Time setting

Switch inputs S1 and S2 have a pull-up resistor to facilitate the use of single-pole, single-throw contacts. A debounce circuit is incorporated to protect against contact bounce and parasitic voltages.

Set enable

Inputs S1 and S2 are enabled by connecting ENABLE to V_{DD} or disabled by connecting to V_{SS}.

Set hours

When S1 is connected to V_{SS} the hours displayed advances by one and after one second continues with one advance per second until S1 is released (auto-increment).

Set minutes

When S2 is connected to V_{SS} the time displayed in minutes advances by one and after one second continues with one advance per second until S2 is released (auto-increment). In addition to minute correction, the seconds counter is reset to zero.

Segment test/reset

When S1 and S2 are connected to V_{SS}, all LCD segments are switched ON. Releasing switches S1 and S2 resets the display. No reset occurs when DATA is connected to V_{SS} (overlapping S1 and S2).

Test mode

When TS is connected to V_{DD}, the device is in normal operating mode. When connecting TS to V_{SS} all counters (seconds, minutes and hours) are stopped, allowing quick testing of the display via S1 and S2 (debounce and auto-increment times are 64 times faster). TS has a pull-up resistor but for reasons of safety it should be connected to V_{DD}.

EEPROM

V_{PP} has a pull-up resistor but for reasons of safety it should be connected to V_{DD}.

LCD voltage programming

To enable LCD voltage programming, SEL is set to open-circuit and a level of $V_{DD} - 5$ V is applied to V_{PP} (see Fig.6). The first pulse (t_E) applied to the DATA input clears the EEPROM to give the lowest voltage output. Further pulses (t_L) will increment the output voltage by steps of typically 150 mV (T_{amb} = 25 °C). For programming, measure $V_{DD} - V_{SS}$ and apply a store pulse (t_W) when the required value is reached. If the maximum number of steps (n = 31) is reached and an additional pulse is applied the voltage will return to the lowest value.

Time calibration

To compensate for the tolerance in the quartz crystal frequency which has been positively offset (nominal deviation $+60 \times 10^{-6}$) by capacitors at the oscillator input and output, a number (n) of 262144 Hz are inhibited every second of operation.

The number (n) is stored in a non-volatile memory which is achieved by the following steps (see Fig.6):

1. Set SEL to V_{SS} and a level of $V_{DD} - 5$ V to V_{PP}
2. The quartz-frequency deviation $\Delta f/f$ is measured and (n) is calculated (see Table 1)
3. A first pulse t_E is applied to the DATA input clears the EEPROM to give the highest backplane frequency
4. The calculated pulses (n) are entered in (t_H, t_L). If the maximum backplane period is reached and an additional pulse is applied the period will return to the lowest value.
5. The backplane period is controlled and when correct fixed by applying the store pulse t_W
6. Release SEL and V_{PP}.

Table 1 Time calibration ($\Delta t = 7.63$ µs; SEL at V_{SS})

OSCILLATOR-FREQUENCY DEVIATION $\Delta f/f$ ($\times 10^{-6}$)	NUMBER OF PULSES (n)	BACKPLANE PERIOD (ms)
0	0	15.625
+3.8	1	15.633
+7.6	2	15.641
+11.4	3	15.648
.	.	.
.	.	.
.	.	.
+117.8	31	15.861

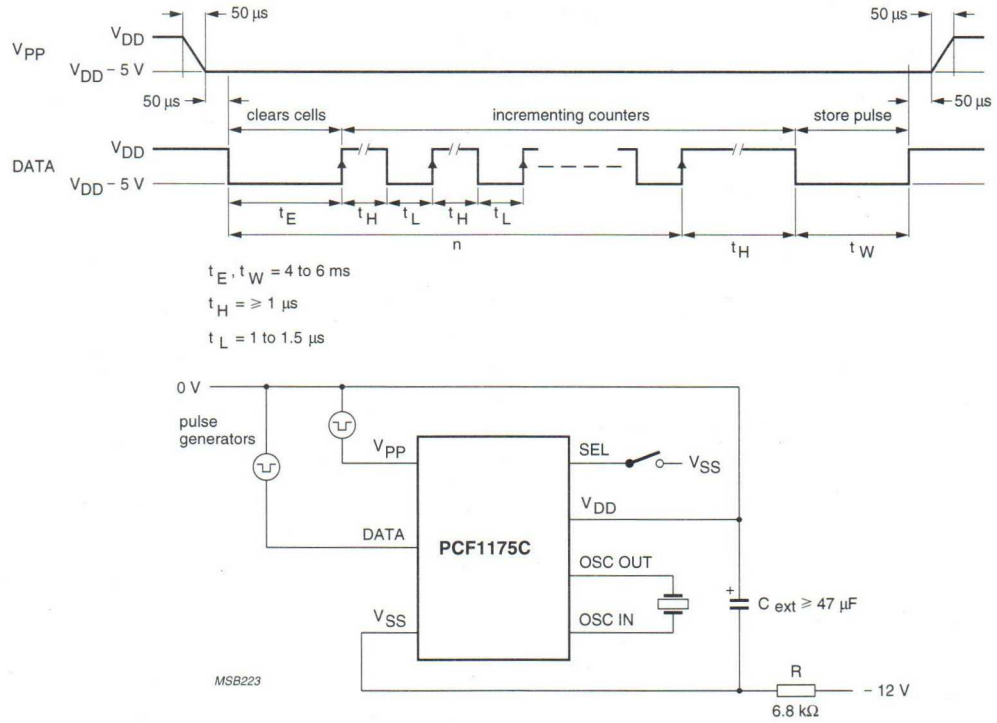


Fig.6 Programming diagram.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	with respect to V_{SS}	–	8	V
I_{DD}	supply current	V_{SS} = 0 V; note 1	–	3	mA
V_I	input voltage	all pins except V_{PP} and DATA	−0.3	V_{DD} + 0.3	V
		pins V_{PP} and DATA	−3	V_{DD} + 0.3	V
T_{amb}	operating ambient temperature		−40	+85	°C
T_{stg}	storage temperature		−55	+125	°C

Note

1. Connecting the supply voltage with reverse polarity, will not harm the circuit, provided the current is limited to 10 mA by an external resistor.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advisable to take handling precautions appropriate to handling MOS devices. Advice can be found in *"Data Handbook IC16, General, Handling MOS Devices"*.

CHARACTERISTICS

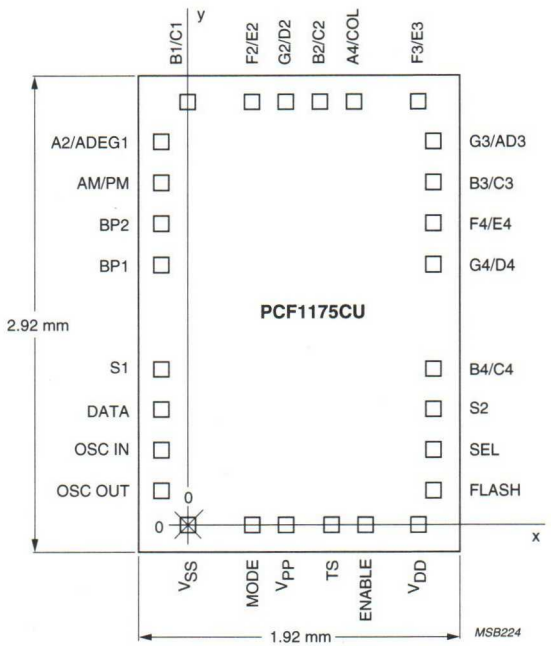
V_{DD} = 3 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; crystal: f = 4.194304 MHz; R_s = 50 Ω; C_L = 12 pF; maximum frequency tolerance = $\pm 30 \times 10^{-6}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	voltage regulator programmed to 4.5 V at T_{amb} = 25 °C	3	–	6	V
ΔV_{DD}	supply voltage variation	S1 or S2 closed	–	–	50	mV
TC	supply voltage variation due to temperature		–	−0.35	–	%/K
		V_{DD} = 4.5 V	–	−16	–	mV/K
I_{DD}	supply current	note 1	700	950	–	µA
C_{EXT}	capacitance	external capacitor	47	–	–	µF
Oscillator						
t_{osc}	start time		–	–	200	ms
Δf/f	frequency deviation	nominal n = 0	0	60×10^{-6}	110×10^{-6}	
Δf/f	frequency stability	ΔV_{DD} = 100 mV	–	–	1×10^{-6}	
R_{fb}	feedback resistance		300	1000	3000	kΩ
C_i	input capacitance		–	16	–	pF
C_o	output capacitance		–	27	–	pF
Inputs						
R_O	pull-up resistance	S1, S2, TS, SEL and DATA	45	90	180	kΩ
R_O	pull-up/pull-down resistance	MODE	100	300	1000	kΩ
I_{IL}	leakage current	ENABLE, FLASH	–	–	2	µA
t_d	debounce time	S1 and S2 only	30	65	100	ms
V_{PP} programming voltage						
I_{O2}	output current	$V_{PP} = V_{DD} - 5$ V	70	–	700	µA
		during programming	–	500	–	µA
Backplane (high and low levels)						
R_{BP}	output resistance	±100 µA	–	–	3	kΩ
Segment						
R_{SEG}	output resistance	±100 µA	–	–	5	kΩ
LCD						
$V_{offset(DC)}$	DC offset voltage	200 kΩ/1 nF	–	–	50	mV

Note

1. A suitable resistor (R) must be selected (example):
   a) V_{DD} = 5 V; R max. (12 V − 5 V)/700 µA = 10 kΩ.
   b) V_{DD} = 5 V; R typ. (12 V − 5 V)/900 µA = 7.8 kΩ (more reserve).
   c) I_{DD} must not exceed 3 mA.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 5.61 mm^2.
Bonding pad dimensions: 110 µm × 110 µm.
Chip thickness: 381 ±25 µm.

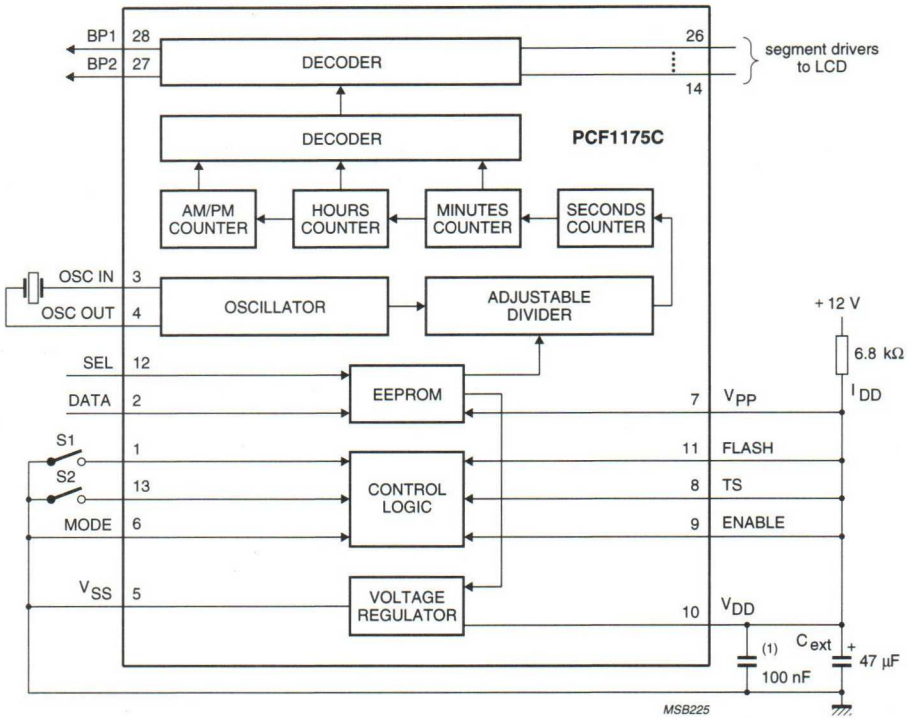
Fig.7 Bonding pad locations, PCF1175CU; 28 terminals.

Table 2 Bonding pad locations (dimensions in μm)

All x/y coordinates are referenced to the bottom left pad (V_{SS}), see Fig.7.

PAD	x	y	PAD	x	y
S1	−138	881	G4/D4	1438	1588
DATA	−138	639	F4/E4	1438	1808
OSC IN	−138	408	B3/C3	1438	2028
OSC OUT	−138	188	G3/AD3	1438	2248
V_{SS}	0	0	F3/E3	1400	2476
MODE	383	0	A4/COL	1000	2476
V_{PP}	583	0	B2/C2	800	2476
TS	846	0	G2/D2	600	2476
ENABLE	1046	0	F2/E2	400	2476
V_{DD}	1352	0	B1/C1	0	2476
FLASH	1438	188	A2/ADEG1	−138	2248
SEL	1438	408	AM/PM	−138	2028
S2	1438	628	BP2	−138	1808
B4/C4	1438	848	BP1	−138	1588
chip corner (max. value)	−355	−175			

APPLICATION INFORMATION



(1) To be placed close to the IC.

Fig.8 Typical application diagram.

4-digit duplex LCD car clock PCF1178C

FEATURES

- Internal voltage regulator is electrically programmable for various LCD voltages
- Time calibration is electrically programmable (no trimming capacitor required)
- LCD voltage adjusts with temperature for good contrast
- 4.19 MHz oscillator
- 12-hour or 24-hour mode
- Operating ambient temperature: –40 to +85 °C
- 28-lead plastic SMD (SO28)
- 1 Hz set mode.

GENERAL DESCRIPTION

The PCF1178C is a single chip, 4.19 MHz CMOS car clock circuit providing hours, minutes and seconds functions. It is designed to drive a 4-digit duplex liquid crystal display (LCD).

Two external single-pole, single-throw switches will accomplish all time setting functions. Time calibration and voltage regulator are electrically programmable via an on-chip EEPROM. The circuit is battery-operated via an internal voltage regulator and an external resistor.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF1178CT	SO28	plastic small outline package; 28 leads; body width 7.5 mm[1]	SOT136-1
PCF1178CU	–	uncased chip in tray[2]	–
PCF1178CU/10	–	chip-on-film frame carrier (FFC)[2]	–
PCF1178CU/5	–	unsawn wafer[2]	–

Notes

1. See Fig.1 and Chapter "Package outline" for pin layout and package details.
2. See Chapter "Chip dimensions and bonding pad locations" for pad layout and package details.

PINNING

SYMBOL	PIN	DESCRIPTION
BP1	1	backplane 1
BP2	2	backplane 2
AM/PM	3	segment driver
A2/ADEG1	4	segment driver
B1/C1	5	segment driver
F2/E2	6	segment driver
G2/D2	7	segment driver
B2/C2	8	segment driver
A4/COL	9	segment driver
F3/E3	10	segment driver
G3/AD3	11	segment driver
B3/C3	12	segment driver
F4/E4	13	segment driver
G4/D4	14	segment driver
B4/C4	15	segment driver
S2	16	minute adjustment input
SEL	17	EEPROM select input
FLASH	18	colon option input
V_{DD}	19	positive supply voltage
ENABLE	20	enable input (for S1 and S2)
TS	21	test speed-up mode input
V_{PP}	22	programming voltage input
MODE	23	12/24-hour mode select input
V_{SS}	24	negative supply voltage
OSC OUT	25	oscillator output
OSC IN	26	oscillator input
DATA	27	EEPROM data input
S1	28	hour adjustment input

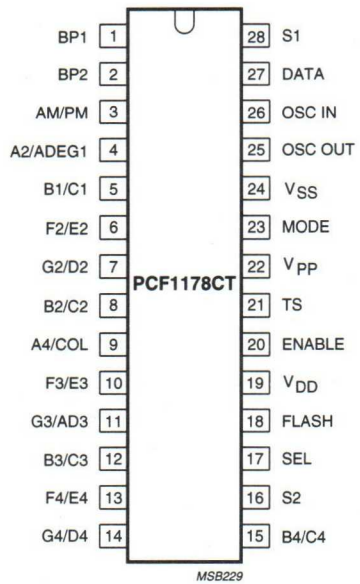


Fig.1 Pin configuration, PCF1178CT, (SO28).

FUNCTIONAL DESCRIPTION AND TESTING

Outputs

The circuit outputs 1 : 2 multiplexed data (duplex) to the LCD. Generation of BP1 and BP2 (three-level backplane signals) and the output signals are shown in Fig.4.

The average voltages across the segments are:

1. $V_{ON(RMS)} = 0.79\ V_{DD}$
2. $V_{OFF(RMS)} = 0.35\ V_{DD}$.

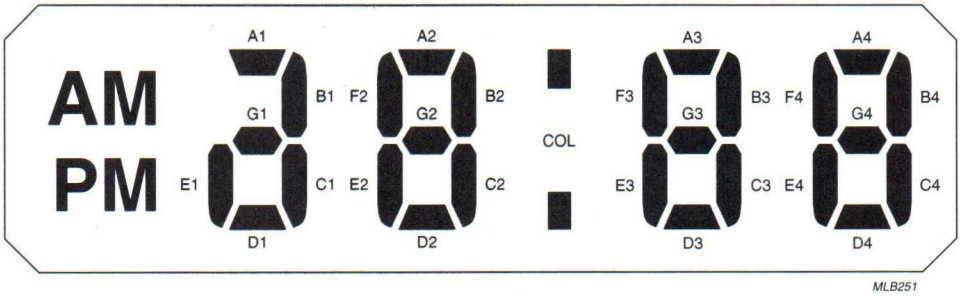
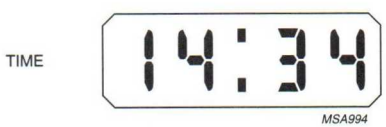


Fig.2 Segment designation of LCD.



(a)

a. 12-hour mode.



(b)

b. 24-hour mode.

Fig.3 Typical displays.

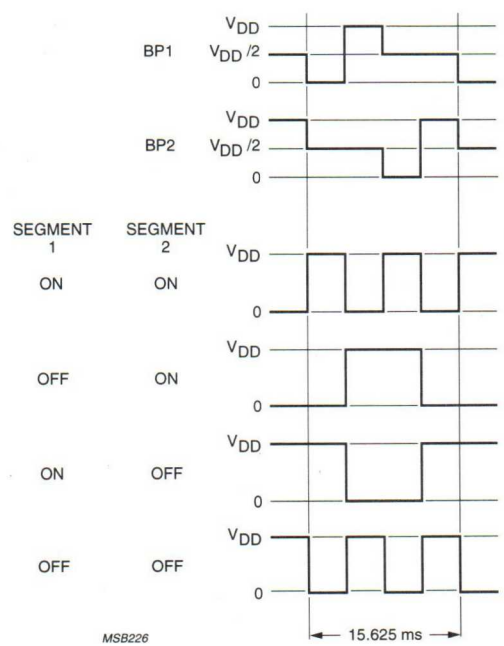


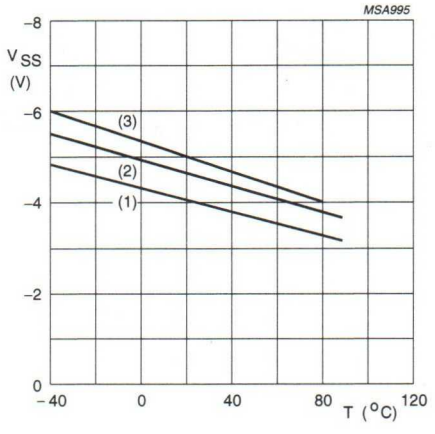
Fig.4 Backplane and output signals.

LCD voltage (see Fig.5)

The adjustable voltage regulator controls the supply voltage (see Section "LCD voltage programming") in relation to temperature for good contrast, for example when V_{DD} = 4.5 V at +25 °C, then:

V_{DD} = 3 to 4 V at +85 °C.

V_{DD} = 5 to 6 V at −40 °C.



(1) Programmed to 4.0 V at 25 °C (value within the specified operating range).
(2) Programmed to 4.5 V at 25 °C (value within the specified operating range).
(3) Programmed to 5.0 V at 25 °C (value within the specified operating range).

Fig.5 Regulated voltage as a function of temperature (typical).

12/24-hour mode

Operation in 12-hour or 24-hour mode is selected by connecting MODE to V_{DD} or V_{SS} respectively. If MODE is left open-circuit and a reset occurs, the mode will change from 12-hour to 24-hour mode or vice versa.

Power-on

After connecting the supply, the start-up mode is:

MODE connected to V_{DD}: 12-hour mode, 1:00 AM.

MODE connected to V_{SS}: 24-hour mode, 0:00.

MODE left open-circuit: 24-hour mode, 0:00 or 1:00.

Colon

If FLASH is connected to V_{DD} the colon pulses at 0.5 Hz. If FLASH is connected to V_{SS} the colon is static.

Time setting

Switch inputs S1 and S2 have a pull-up resistor to facilitate the use of single-pole, single-throw contacts. A debounce circuit is incorporated to protect against contact bounce and parasitic voltages.

Set enable

Inputs S1 and S2 are enabled by connecting ENABLE to V_{DD} or disabled by connecting to V_{SS}.

Set hours

When S1 is connected to V_{SS} the hours displayed advances by one and after one second continues with one advance per second until S1 is released (auto-increment).

Set minutes

When S2 is connected to V_{SS} the time displayed in minutes advances by one and after one second continues with two advances per second until S2 is released (auto-increment). In addition to minute correction, the seconds counter is reset to zero.

Segment test/reset

When S1 and S2 are connected to V_{SS}, all LCD segments are switched ON. Releasing switches S1 and S2 resets the display. No reset occurs when DATA is connected to V_{SS} (overlapping S1 and S2).

Test mode

When TS is connected to V_{DD}, the device is in normal operating mode. When connecting TS to V_{SS} all counters (seconds, minutes and hours) are stopped, allowing quick testing of the display via S1 and S2 (debounce and auto-increment times are 64 times faster). TS has a pull-up resistor but for reasons of safety it should be connected to V_{DD}.

EEPROM

V_{PP} has a pull-up resistor but for reasons of safety it should be connected to V_{DD}.

LCD voltage programming

To enable LCD voltage programming, SEL is set to open-circuit and a level of $V_{DD} - 5$ V is applied to V_{PP} (see Fig.6). The first pulse (t_E) applied to the DATA input clears the EEPROM to give the lowest voltage output. Further pulses (t_L) will increment the output voltage by steps of typically 150 mV (T_{amb} = 25 °C). For programming, measure $V_{DD} - V_{SS}$ and apply a store pulse (t_W) when the required value is reached. If the maximum number of steps (n = 31) is reached and an additional pulse is applied the voltage will return to the lowest value.

Time calibration

To compensate for the tolerance in the quartz crystal frequency which has been positively offset (nominal deviation $+60 \times 10^{-6}$) by capacitors at the oscillator input and output, a number (n) of 262144 Hz pulses are inhibited every second of operation.

The number (n) is stored in a non-volatile memory which is achieved by the following steps (see Fig.6):

1. Set SEL to V_{SS} and a level of $V_{DD} - 5$ V to V_{PP}
2. The quartz-frequency deviation $\Delta f/f$ is measured and (n) is calculated (see Table 1)
3. A first pulse t_E is applied to the DATA input clears the EEPROM to give the highest backplane frequency
4. The calculated pulses (n) are entered in (t_H, t_L). If the maximum backplane period is reached and an additional pulse is applied the period will return to the lowest value.
5. The backplane period is controlled and when correct fixed by applying the store pulse t_W
6. Release SEL and VPP.

Table 1 Time calibration (Δt = 7.63 µs; SEL at V_{SS})

OSCILLATOR-FREQUENCY DEVIATION $\Delta f/f$ ($\times 10^{-6}$)	NUMBER OF PULSES (n)	BACKPLANE PERIOD (ms)
0	0	15.625
+3.8	1	15.633
+7.6	2	15.641
+11.4	3	15.648
.	.	.
.	.	.
.	.	.
+117.8	31	15.861

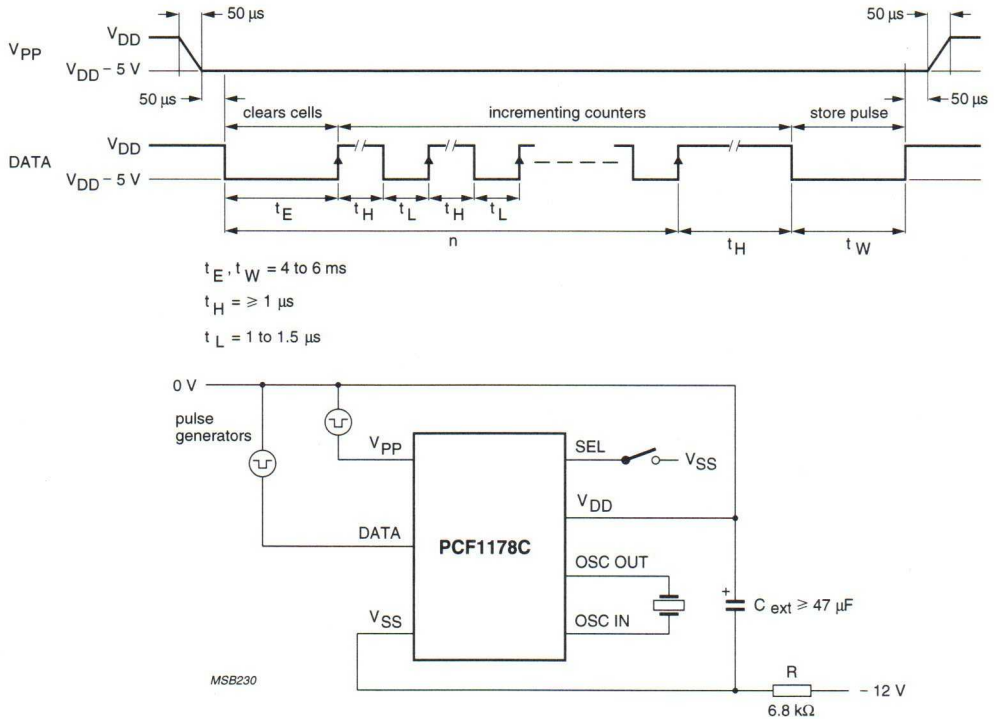


Fig.6 Programming diagram.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	with respect to V_{SS}	–	8	V
I_{DD}	supply current	V_{SS} = 0 V; note 1	–	3	mA
V_I	input voltage	all pins except V_{PP} and DATA	−0.3	V_{DD} + 0.3	V
		pins V_{PP} and DATA	−3	V_{DD} + 0.3	V
T_{amb}	operating ambient temperature		−40	+85	°C
T_{stg}	storage temperature		−55	+125	°C

Note

1. Connecting the supply voltage with reverse polarity, will not harm the circuit, provided the current is limited to 10 mA by an external resistor.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advisable to take handling precautions appropriate to handling MOS devices. Advice can be found in *"Data Handbook IC16, General, Handling MOS Devices"*.

CHARACTERISTICS

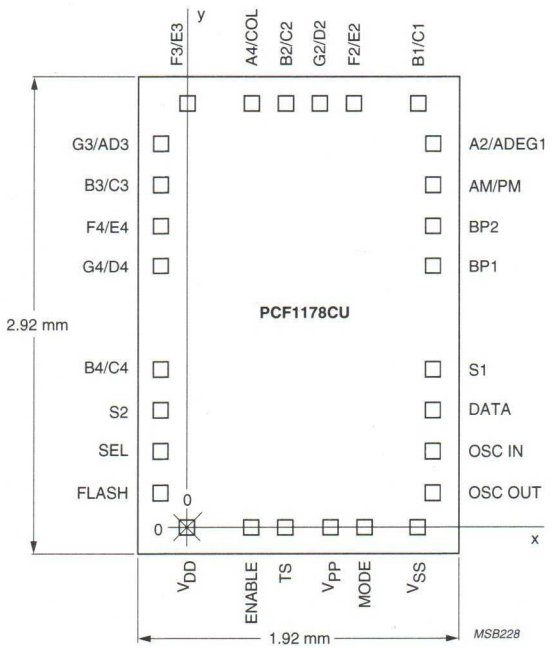
V_{DD} = 3 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; crystal: f = 4.194304 MHz; R_s = 50 Ω; C_L = 12 pF; maximum frequency tolerance = $\pm 30 \times 10^{-6}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	voltage regulator programmed to 4.5 V at T_{amb} = 25 °C	3	–	6	V
ΔV_{DD}	supply voltage variation	S1 or S2 closed	–	–	50	mV
TC	supply voltage variation due to temperature		–	−0.35	–	%/K
		V_{DD} = 4.5 V	–	−16	–	mV/K
I_{DD}	supply current	note 1	700	950	–	µA
C_{EXT}	capacitance	external capacitor	47	–	–	µF
Oscillator						
t_{osc}	start time		–	–	200	ms
Δf/f	frequency deviation	nominal n = 0	0	60×10^{-6}	110×10^{-6}	
Δf/f	frequency stability	ΔV_{DD} = 100 mV	–	–	1×10^{-6}	
R_{fb}	feedback resistance		300	1000	3000	kΩ
C_i	input capacitance		–	16	–	pF
C_o	output capacitance		–	27	–	pF
Inputs						
R_O	pull-up resistance	S1, S2, TS, SEL and DATA	45	90	180	kΩ
R_O	pull-up/pull-down resistance	MODE	100	300	1000	kΩ
I_{IL}	leakage current	ENABLE, FLASH	–	–	2	µA
t_d	debounce time	S1 and S2 only	30	65	100	ms
V_{PP} programming voltage						
I_{O2}	output current	$V_{PP} = V_{DD} - 5$ V	70	–	700	µA
		during programming	–	500	–	µA
Backplane (high and low levels)						
R_{BP}	output resistance	±100 µA	–	–	3	kΩ
Segment						
R_{SEG}	output resistance	±100 µA	–	–	5	kΩ
LCD						
$V_{offset(DC)}$	DC offset voltage	200 kΩ/1 nF	–	–	50	mV

Note

1. A suitable resistor (R) must be selected (example):
   a) V_{DD} = 5 V; R max. (12 V − 5 V)/700 µA = 10 kΩ.
   b) V_{DD} = 5 V; R typ. (12 V − 5 V)/900 µA = 7.8 kΩ (more reserve).
   c) I_{DD} must not exceed 3 mA.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 5.61 mm^2.
Bonding pad dimensions: 110 µm × 110 µm.
Chip thickness: 381 ±25 µm.

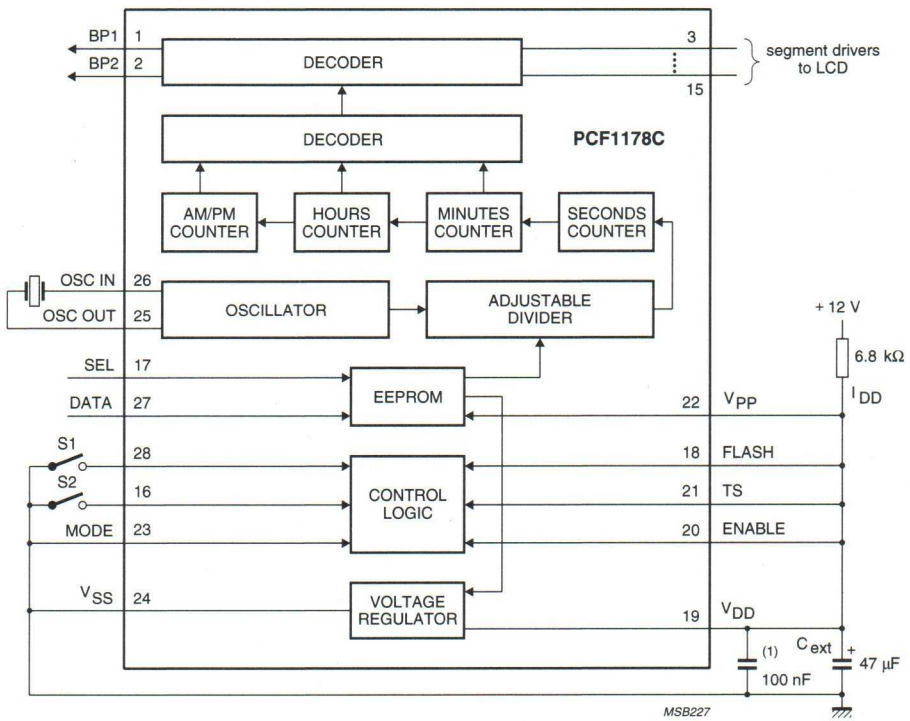
Fig.7 Bonding pad locations, PCF1178CU; 28 terminals.

Table 2 Bonding pad locations (dimensions in μm)

All x/y coordinates are referenced to the bottom left pad (V_{DD}), see Fig.7.

PAD	x	y	PAD	x	y
S1	1490	881	G4/D4	−86	1588
DATA	1490	639	F4/E4	−86	1808
OSC IN	1490	408	B3/C3	−86	2028
OSC OUT	1490	188	G3/AD3	−86	2248
V_{SS}	1352	0	F3/E3	−48	2476
MODE	969	0	A4/COL	352	2476
V_{PP}	770	0	B2/C2	552	2476
TS	506	0	G2/D2	752	2476
ENABLE	306	0	F2/E2	952	2476
V_{DD}	0	0	B1/C1	1352	2476
FLASH	−86	188	A2/ADEG1	1490	2248
SEL	−86	408	AM/PM	1490	2028
S2	−86	628	BP2	1490	1808
B4/C4	−86	848	BP1	1490	1588
chip corner (max. value)	−305	−175			

APPLICATION INFORMATION



(1) To be placed close to the IC.

Fig.8 Typical application diagram.

4-digit duplex LCD car clock PCF1179C

FEATURES

- Internal voltage regulator is electrically programmable for various LCD voltages
- Time calibration is electrically programmable (no trimming capacitor required)
- LCD voltage adjusts with temperature for good contrast
- 4.19 MHz oscillator
- 12-hour or 24-hour mode
- Operating ambient temperature: –40 to +85 °C
- 28-lead plastic SMD (SO28)
- 4 Hz set mode.

GENERAL DESCRIPTION

The PCF1179C is a single chip, 4.19 MHz CMOS car clock circuit providing hours, minutes and seconds functions. It is designed to drive a 4-digit duplex liquid crystal display (LCD).

Two external single-pole, single-throw switches will accomplish all time setting functions. Time calibration and voltage regulator are electrically programmable via an on-chip EEPROM. The circuit is battery-operated via an internal voltage regulator and an external resistor.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF1179CT	SO28	plastic small outline package; 28 leads; body width 7.5 mm[1]	SOT136-1
PCF1179CU	–	uncased chip in tray[2]	–
PCF1179CU/10	–	chip-on-film frame carrier (FFC)[2]	–

Notes

1. See Fig.1 and Chapter "Package outline" for pin layout and package details.
2. See Chapter "Chip dimensions and bonding pad locations" for pad layout and package details.

PINNING

SYMBOL	PIN	DESCRIPTION
S1	1	hour adjustment input
DATA	2	EEPROM data input
OSC IN	3	oscillator input
OSC OUT	4	oscillator output
V_{SS}	5	negative supply voltage
MODE	6	12/24-hour mode select input
V_{PP}	7	programming voltage input
TS	8	test speed-up mode input
ENABLE	9	enable input (for S1 and S2)
V_{DD}	10	positive supply voltage
FLASH	11	colon option input
SEL	12	EEPROM select input
S2	13	minute adjustment input
B4/C4	14	segment driver
G4/D4	15	segment driver
F4/E4	16	segment driver
B3/C3	17	segment driver
G3/AD3	18	segment driver
F3/E3	19	segment driver
A4/COL	20	segment driver
B2/C2	21	segment driver
G2/D2	22	segment driver
F2/E2	23	segment driver
B1/C1	24	segment driver
A2/ADEG1	25	segment driver
AM/PM	26	segment driver
BP2	27	backplane 2
BP1	28	backplane 1

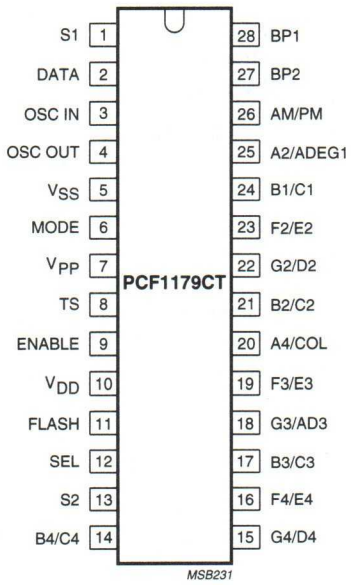


Fig.1 Pin configuration, PCF1179CT, (SO28).

FUNCTIONAL DESCRIPTION AND TESTING

Outputs

The circuit outputs 1 : 2 multiplexed data (duplex) to the LCD. Generation of BP1 and BP2 (three-level backplane signals) and the output signals are shown in Fig.4.

The average voltages across the segments are:

1. $V_{ON(RMS)} = 0.79\ V_{DD}$
2. $V_{OFF(RMS)} = 0.35\ V_{DD}$.

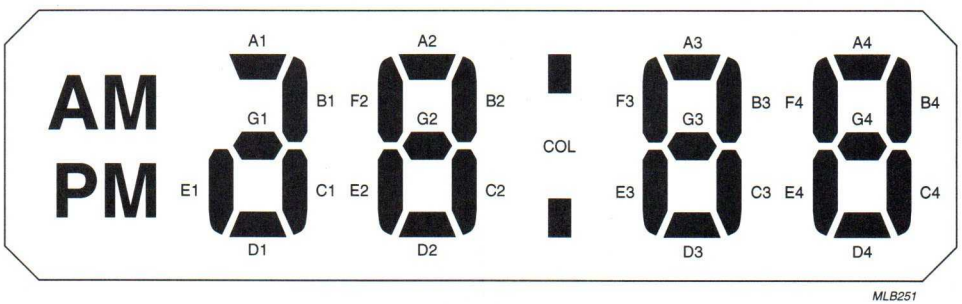
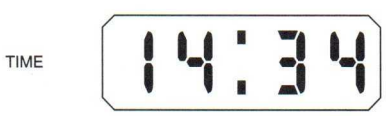


Fig.2 Segment designation of LCD.



(a)

a. 12-hour mode.



(b)

b. 24-hour mode.

Fig.3 Typical displays.

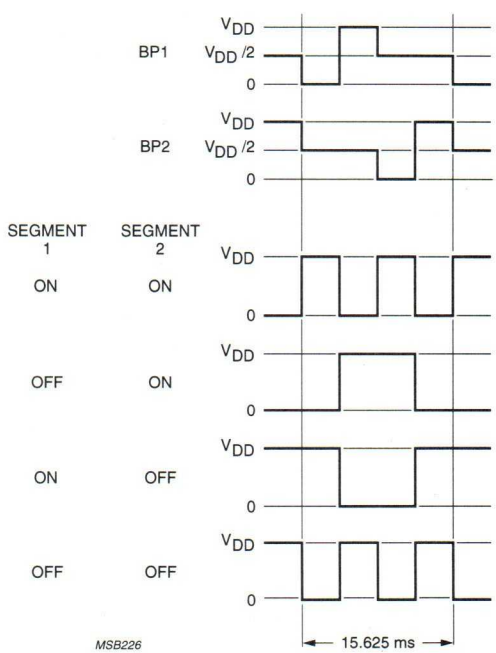


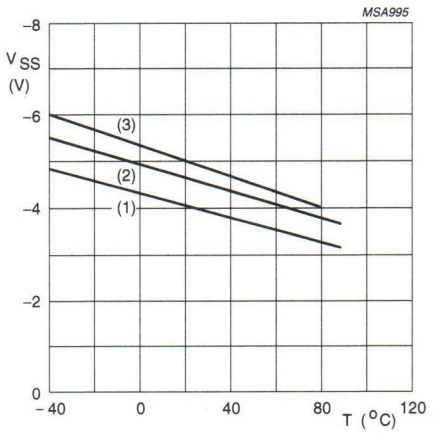
Fig.4 Backplane and output signals.

LCD voltage (see Fig.5)

The adjustable voltage regulator controls the supply voltage (see Section "LCD voltage programming") in relation to temperature for good contrast, for example when V_{DD} = 4.5 V at +25 °C, then:

V_{DD} = 3 to 4 V at +85 °C.

V_{DD} = 5 to 6 V at −40 °C.



(1) Programmed to 4.0 V at 25 °C (value within the specified operating range).
(2) Programmed to 4.5 V at 25 °C (value within the specified operating range).
(3) Programmed to 5.0 V at 25 °C (value within the specified operating range).

Fig.5 Regulated voltage as a function of temperature (typical).

12/24-hour mode

Operation in 12-hour or 24-hour mode is selected by connecting MODE to V_{DD} or V_{SS} respectively. If MODE is left open-circuit and a reset occurs, the mode will change from 12-hour to 24-hour mode or vice versa.

Power-on

After connecting the supply, the start-up mode is:

MODE connected to V_{DD}: 12-hour mode, 1:00 AM.

MODE connected to V_{SS}: 24-hour mode, 0:00.

MODE left open-circuit: 24-hour mode, 0:00 or 1:00.

Colon

If FLASH is connected to V_{DD} the colon pulses at 1 Hz. If FLASH is connected to V_{SS} the colon is static.

Time setting

Switch inputs S1 and S2 have a pull-up resistor to facilitate the use of single-pole, single-throw contacts. A debounce circuit is incorporated to protect against contact bounce and parasitic voltages.

Set enable

Inputs S1 and S2 are enabled by connecting ENABLE to V_{DD} or disabled by connecting to V_{SS}.

Set hours

When S1 is connected to V_{SS} the hours displayed advances by one and after one second continues with four advances per second until S1 is released (auto-increment). An overflow in the hour counter must not have an influence on the minute counter.

Set minutes

When S2 is connected to V_{SS} the time displayed in minutes advances by one and after one second continues with four advances per second until S2 is released (auto-increment). In addition to minute correction, the seconds counter is reset to zero. An overflow in the minute counter must not have an influence on the hour counter.

Segment test/reset

When S1 and S2 are connected to V_{SS}, all LCD segments are switched ON. Releasing switches S1 and S2 resets the display. No reset occurs when DATA is connected to V_{SS} (overlapping S1 and S2).

Test mode

When TS is connected to V_{DD}, the device is in normal operating mode. When connecting TS to V_{SS} all counters (seconds, minutes and hours) are stopped, allowing quick testing of the display via S1 and S2 (debounce and auto-increment times are 64 times faster). TS has a pull-up resistor but for reasons of safety it should be connected to V_{DD}.

EEPROM

V_{PP} has a pull-up resistor but for reasons of safety it should be connected to V_{DD}.

LCD voltage programming

To enable LCD voltage programming, SEL is set to open-circuit and a level of $V_{DD} - 5$ V is applied to V_{PP} (see Fig.6). The first pulse (t_E) applied to the DATA input clears the EEPROM to give the lowest voltage output. Further pulses (t_L) will increment the output voltage by steps of typically 150 mV (T_{amb} = 25 °C). For programming, measure $V_{DD} - V_{SS}$ and apply a store pulse (t_W) when the required value is reached. If the maximum number of steps (n = 31) is reached and an additional pulse is applied the voltage will return to the lowest value.

Time calibration

To compensate for the tolerance in the quartz crystal frequency which has been positively offset (nominal deviation $+60 \times 10^{-6}$ by capacitors at the oscillator input and output, a number (n) of 262144 Hz pulses are inhibited every second of operation.

The number (n) is stored in a non-volatile memory which is achieved by the following steps (see Fig.6):

1. Set SEL to V_{SS} and a level of $V_{DD} - 5$ V to V_{PP}
2. The quartz-frequency deviation $\Delta f/f$ is measured and (n) is calculated (see Table 1)
3. A first pulse t_E is applied to the DATA input clears the EEPROM to give the highest backplane frequency
4. The calculated pulses (n) are entered in (t_H, t_L). If the maximum backplane period is reached and an additional pulse is applied the period will return to the lowest value.
5. The backplane period is controlled and when correct fixed by applying the store pulse t_W
6. Release SEL and V_{PP}.

Table 1 Time calibration ($\Delta t = 7.63$ µs; SEL at V_{SS})

OSCILLATOR-FREQUENCY DEVIATION $\Delta f/f$ ($\times 10^{-6}$)	NUMBER OF PULSES (n)	BACKPLANE PERIOD (ms)
0	0	15.625
+3.8	1	15.633
+7.6	2	15.641
+11.4	3	15.648
.	.	.
.	.	.
.	.	.
+117.8	31	15.861

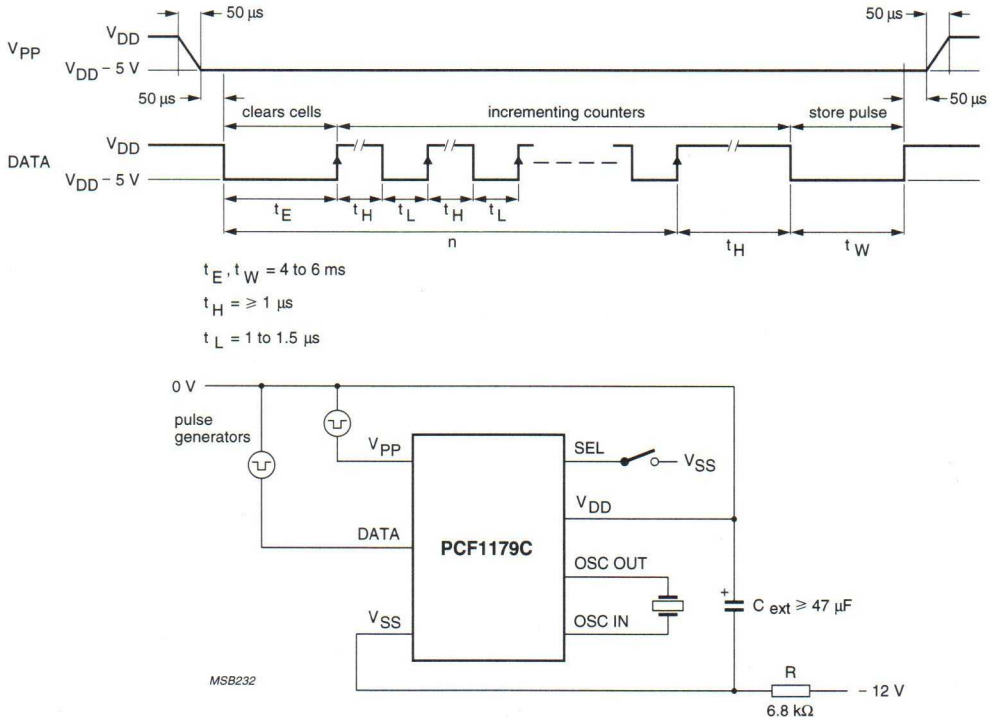


Fig.6 Programming diagram.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	with respect to V_{SS}	–	8	V
I_{DD}	supply current	V_{SS} = 0 V; note 1	–	3	mA
V_I	voltage range	all pins except V_{PP} and DATA	−0.3	V_{DD} + 0.3	V
		pins V_{PP} and DATA	−3	V_{DD} + 0.3	V
T_{amb}	operating ambient temperature		−40	+85	°C
T_{stg}	storage temperature		−55	+125	°C

Note

1. Connecting the supply voltage with reverse polarity, will not harm the circuit, provided the current is limited to 10 mA by an external resistor.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advisable to take handling precautions appropriate to handling MOS devices. Advice can be found in *"Data Handbook IC16, General, Handling MOS Devices"*.

CHARACTERISTICS

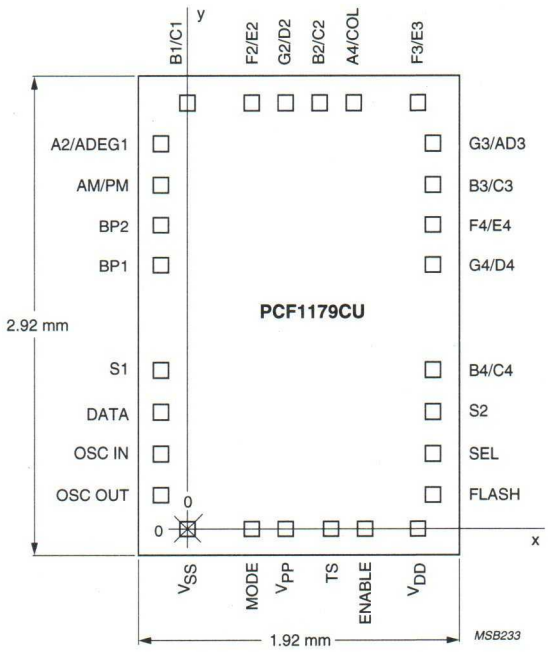
V_{DD} = 3 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; crystal: f = 4.194304 MHz; R_s = 50 Ω; C_L = 12 pF; maximum frequency tolerance = $\pm 30 \times 10^{-6}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	voltage regulator programmed to 4.5 V at T_{amb} = 25 °C	3	–	6	V
ΔV_{DD}	supply voltage variation	S1 or S2 closed	–	–	50	mV
TC	supply voltage variation due to temperature		–	−0.35	–	%/K
		V_{DD} = 4.5 V	–	−16	–	mV/K
I_{DD}	supply current	note 1	700	950	–	µA
C_{EXT}	capacitance	external capacitor	47	–	–	µF
Oscillator						
t_{osc}	start time		–	–	200	ms
Δf/f	frequency deviation	nominal n = 0	0	60×10^{-6}	110×10^{-6}	
Δf/f	frequency stability	ΔV_{DD} = 100 mV	–	–	1×10^{-6}	
R_{fb}	feedback resistance		300	1000	3000	kΩ
C_i	input capacitance		–	16	–	pF
C_o	output capacitance		–	27	–	pF
Inputs						
R_O	pull-up resistance	S1, S2, TS, SEL and DATA	45	90	180	kΩ
R_O	pull-up/pull-down resistance	MODE	100	300	1000	kΩ
I_{IL}	leakage current	ENABLE, FLASH	–	–	2	µA
t_d	debounce time	S1 and S2 only	30	65	100	ms
V_{PP} programming voltage						
I_{O2}	output current	$V_{PP} = V_{DD} - 5$ V	70	–	700	µA
		during programming	–	500	–	µA
Backplane (high and low levels)						
R_{BP}	output resistance	±100 µA	–	–	3	kΩ
Segment						
R_{SEG}	output resistance	±100 µA	–	–	5	kΩ
LCD						
$V_{offset(DC)}$	DC offset voltage	200 kΩ/1 nF	–	–	50	mV

Note

1. A suitable resistor (R) must be selected (example):
   a) V_{DD} = 5 V; R max. (12 V − 5 V)/700 µA = 10 kΩ.
   b) V_{DD} = 5 V; R typ. (12 V − 5 V)/900 µA = 7.8 kΩ (more reserve).
   c) I_{DD} must not exceed 3 mA.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 5.61 mm^2.
Bonding pad dimensions: 110 µm × 110 µm.
Chip thickness: 381 ±25 µm.

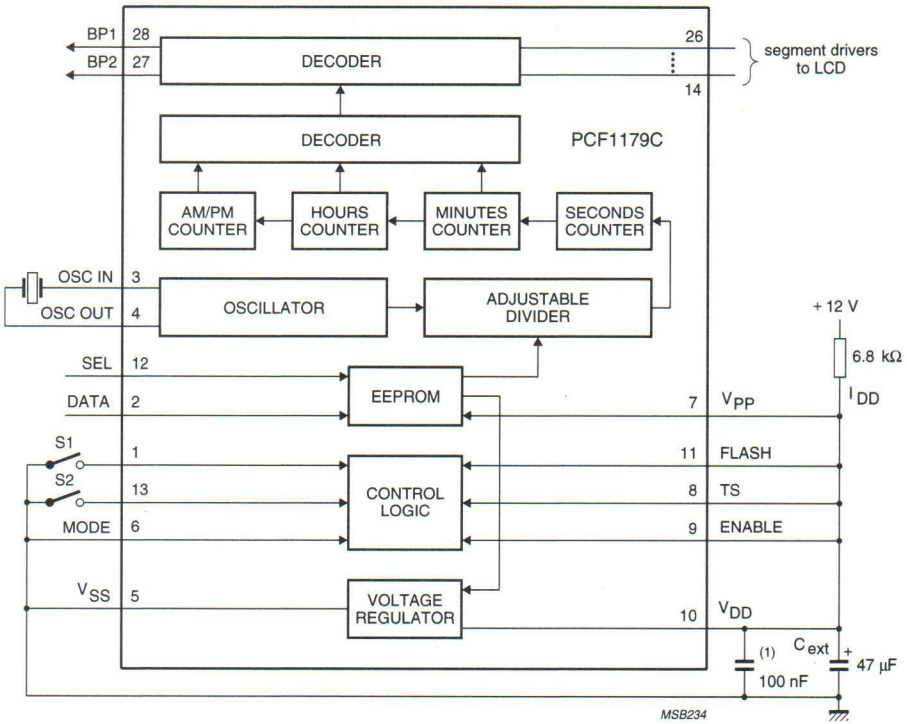
Fig.7 Bonding pad locations, PCF1179CU; 28 terminals.

Table 2 Bonding pad locations (dimensions in μm)

All x/y coordinates are referenced to the bottom left pad (V_{SS}), see Fig.7.

PAD	x	y	PAD	x	y
S1	−138	881	G4/D4	1438	1588
DATA	−138	639	F4/E4	1438	1808
OSC IN	−138	408	B3/C3	1438	2028
OSC OUT	−138	188	G3/AD3	1438	2248
V_{SS}	0	0	F3/E3	1400	2476
MODE	383	0	A4/COL	1000	2476
V_{PP}	583	0	B2/C2	800	2476
TS	846	0	G2/D2	600	2476
ENABLE	1046	0	F2/E2	400	2476
V_{DD}	1352	0	B1/C1	0	2476
FLASH	1438	188	A2/ADEG1	−138	2248
SEL	1438	408	AM/PM	−138	2028
S2	1438	628	BP2	−138	1808
B4/C4	1438	848	BP1	−138	1588
chip corner (max. value)	−355	−175			

APPLICATION INFORMATION



(1) To be mounted close to the IC.

Fig.8 Typical application diagram.

Real-time clock/calendar PCF8563

FEATURES

- Provides year, month, day, weekday, hours, minutes, seconds based on 32.768 kHz quartz crystal
- Century flag
- Wide clock operating voltage: 1.0 - 5.5 V
- Low back-up current typical 0.25 μA @ 3.0 V, 25 °C
- 400 kHz two-wire I²C interface (1.8 - 5.5 V)
- Programmable clock output for peripheral devices (32.768 kHz, 1024 Hz, 32 Hz, 1 Hz)
- Alarm and timer functions
- Low-voltage detector
- Integrated oscillator capacitor
- Internal power-on reset
- I²C slave address: read A3h, write A2h
- Open drain interrupt pin.

GENERAL DESCRIPTION

The PCF8563 is a CMOS real-time clock/calendar optimized for low power consumption. A programmable clock output, interrupt output and voltage low detector are also provided. All address and data are transferred serially via a two-line bidirectional I²C bus. Maximum bus speed is 400 kbit/sec. The built-in word address register is incremented automatically after each written or read data byte.

APPLICATIONS

- Mobile telephones
- Portable instruments
- Fax machines
- Battery powered products.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	Supply voltage operating mode	I²C bus active –40 to +85 °C	1.8	5.5	V
		Clock operating, 25 °C	1.0	5.5	V
I_{DD}	Supply current (Timer and CLKOUT disabled)	f_{SCL} = 100 kHz	–	200	μA
		f_{SCL} = 400 kHz	–	800	μA
		f_{SCL} = 0 Hz: V_{DD} = 5 V, 25 °C	–	1.0	μA
		f_{SCL} = 0 Hz: V_{DD} = 2 V, 25 °C	–	0.75	μA
T_{AMB}	Operating ambient temperature		–40	+85	°C
T_{STG}	Storage temperature		–55	+125	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8563P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCF8563T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

BLOCK DIAGRAM

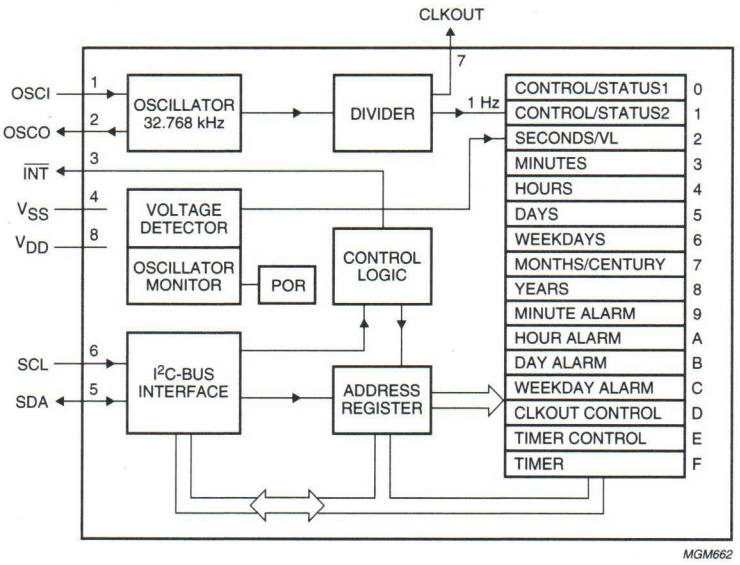


Fig.1 Block diagram PCF8563 real-time clock/calendar.

PINNING INFORMATION

Pin description

SYMBOL	PIN	DESCRIPTION
OSCI	1	Oscillator input
OSCO	2	Oscillator output
$\overline{INT}$	3	Open drain interrupt output (active LOW)
V_{SS}	4	Ground
SDA	5	Serial data I/O
SCL	6	Serial clock input
CLKOUT	7	Clock output
V_{DD}	8	Positive supply

Pinning

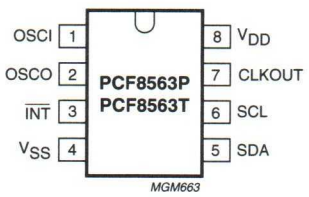


Fig.2 Pinning.

FUNCTIONAL DESCRIPTION

The PCF8563 contains sixteen 8-bit registers with an auto-incrementing address register, an on-chip 32.768 kHz oscillator with one integrated capacitor, a frequency divider which provides the source clock for the real time clock (RTC), a programmable clock output, a timer, an alarm, a voltage-low detector and a 400 kHz I^2C bus interface.

All 16 registers are designed as addressable 8-bit parallel registers although not all bits are implemented. The first two registers (memory address 00, 01) are used as control and/or status registers. The memory addresses 02 through 08 are used as counters for the clock function (seconds up to year counters). Address locations 09 through 0C contain alarm registers which define the conditions for an alarm. Address 0D controls the CLKOUT output frequency. 0E and 0F are the timer control and timer registers, respectively.

The seconds, minutes, hours, days, weekdays, months, years as well as the minute alarm, hour alarm, day alarm and weekday alarm registers are all coded in BCD format.

When one of the RTC registers is read the contents of all counters are frozen. Therefore, faulty reading of the clock/calendar during a carry condition is prevented.

Alarm function modes

By clearing the MSB of one or more of the alarm registers (AE = 'Alarm Enable'), the corresponding alarm condition(s) will be active. In this way an alarm can be generated from once per minute up to once per week. The alarm condition sets the alarm flag, AF. The asserted AF can be used to generate an interrupt ($\overline{INT}$). The AF may only be cleared by software.

Timer

The 8-bit countdown timer at address 0F is controlled by the timer control register at address 0E. The timer control register determines one of 4 source clock frequencies for the timer (4096 Hz, 64 Hz, 1 Hz, or $1/60$ Hz), and enables/disables the timer. The timer counts down from a software-loaded 8-bit binary value. At the end of every countdown, the timer sets the timer flag TF. The TF may only be cleared by software. The asserted TF can be used to generate an interrupt ($\overline{INT}$). The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal which follows the condition of TF. TI/TP is used to control this mode selection. When reading the timer, the current countdown value is returned.

CLKOUT output

A programmable square wave is available at the CLKOUT pin. Operation is controlled by the CLKOUT register at address 0D. Frequencies of 32.768 kHz (default), 1024 Hz, 32 Hz and 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator. CLKOUT is a push-pull output and enabled at power on. If disabled it becomes logic 0.

Reset

The PCF8563 includes an internal reset circuit which is active whenever the oscillator is stopped. In the reset state the I^2C bus logic is initialized and all registers, including the address pointer, are cleared with the exception of bits FE, VL, TD1, TD0, TESTC and AE bits which are set to 1.

Voltage low detector & clock monitor

The PCF8563 has an on-chip voltage low detector. When V_{DD} drops below V_{LOW} the 'Voltage Low' (VL, bit 7 in the seconds register) is set to indicate that the integrity of the clock information is no longer guaranteed. The VL flag can only be cleared by software.

Register organization

Bit positions labelled as 'x' are not implemented, those labelled with '0' should always be written with 0.

ADDRESS	FUNCTION	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00	Control/status 1	TEST1	0	STOP	0	TESTC	0	0	0
01	Control/status 2	0	0	0	TI/TP	AF	TF	AIE	TIE
02	Seconds	VL	4	2	1	8	4	2	1
03	Minutes	x	4	2	1	8	4	2	1
04	Hours	x	x	2	1	8	4	2	1
05	Days	x	x	2	1	8	4	2	1
06	Weekdays	x	x	x	x	x	4	2	1
07	Months/Century	C	x	x	1	8	4	2	1
08	Years	8	4	2	1	8	4	2	1
09	Minute alarm	AE	4	2	1	8	4	2	1
0A	Hour alarm	AE	x	2	1	8	4	2	1
0B	Day alarm	AE	x	2	1	8	4	2	1
0C	Weekday alarm	AE	x	x	x	x	4	2	1
0D	CLKOUT frequency	FE	x	x	x	x	x	FD1	FD0
0E	Timer control	TE	x	x	x	x	x	TD1	TD0
0F	Timer	128	64	32	16	8	4	2	1

Bit assignments

BIT NO.	BIT NAME	BIT VALUE	DESCRIPTION
Control/Status 1		**Address 00**	
3	TESTC	0	Power on reset override facility is disabled. Set to 0 for normal operation.
		1	Power on reset override may be enabled.
5	STOP	0	RTC source clock runs.
		1	All RTC divider chain flip flops are asynchronously set to 0; the RTC clock is stopped (CLKOUT at 32.768 kHz is still available)
7	TEST1	0	Normal mode.
		1	EXT_CLK test mode.
Control/Status 2		**Address 01**	
TIE & AIE		These bits activate or deactivate the generation of an interrupt when TF or AF is asserted, respectively. The interrupt is the logical OR of these two conditions when both AIE and TIE are set	
0	TIE	0	Timer interrupt disabled
		1	Timer interrupt enabled
1	AIE	0	Alarm interrupt disabled
		1	Alarm interrupt enabled

BIT NO.	BIT NAME	BIT VALUE	DESCRIPTION
TF & AF		When an alarm occurs, AF is set to 1. Similarly, at the end of a timer countdown, TF is set to 1.These bits maintain their value until overwritten by software. If both timer and alarm interrupts are required in the application, the source of the interrupt can be determined by reading these bits. To prevent one flag being overwritten while clearing another a logic AND is performed during a write access.	
2	TF	0 (READ)	Timer flag inactive.
		1 (READ)	Timer flag active.
		0 (WRITE)	Timer flag is cleared.
		1 (WRITE)	Timer flag remains unchanged.
3	AF	0 (READ)	Alarm flag inactive.
		1 (READ)	Alarm flag active.
		0 (WRITE)	Alarm flag is cleared.
		1 (WRITE)	Alarm flag remains unchanged.
4	TI/TP	0	$\overline{INT}$ is active when TF is active (subject to the status of TIE).
		1	$\overline{INT}$ pulses active according to table 1(subject to the status of TIE). Note that if AF and AIE are active then $\overline{INT}$ will be permanently active.
Seconds & VL		**Address 02**	
6..0	Seconds	00 - 59	This register holds the current seconds coded in BCD format. Example: seconds register contains 'x1011001' = 59 seconds.
7	VL	0	Clock integrity is guaranteed.
		1	Integrity of the clock information is no longer guaranteed.
Minutes		**Address 03**	
6..0	Minutes	00 - 59	This register holds the current minutes coded in BCD format.
Hours		**Address 04**	
5..0	Hours	00 - 23	This register holds the current hours coded in BCD format.
Days		**Address 05**	
5..0	Days[1]	01 - 31	This register holds the current day coded in BCD format.
Weekdays		**Address 06**	
2..0	Weekdays[2]	0 - 6	This register holds the current weekday coded in BCD format, see table 4.
Months & Century		**Address 07**	
4..0	Month	01 - 12	This register holds the current month coded in BCD format, see table 5.
7	Century[2]	0	Indicates the century is 20xx.
		1	Indicates the century is 19xx.
		This bit is toggled when the years register overflows from 99 to 00.	
Years		**Address 08**	
7..0	Years	00 - 99	This register holds the current year coded in BCD format.

BIT NO.	BIT NAME	BIT VALUE	DESCRIPTION
Alarm registers		**Address 09 to 0C**	
		When one or more of these registers is loaded with a valid minute, hour, day or weekday and its corresponding 'Alarm Enable' (AE) is '0', then that information will be compared with the current minute, hour, day and weekday. When all enabled comparisons first match, the 'Alarm Flag' (AF) is set. AF will remain set until cleared by software. Once AF has been cleared it will only be set again when the time increments to match the alarm condition once more. Alarm registers which have their 'Alarm Enable' bit at '1' will be ignored.	
Alarm: Minute		**Address 09**	
6..0	Alarm minutes	00 - 59	This register holds the minute alarm information coded in BCD format.
7	AE	0	Minute alarm is enabled.
		1	Minute alarm is disabled.
Alarm: Hour		**Address 0A**	
5..0	Alarm hours	00 - 23	This register holds the hour alarm information coded in BCD format.
7	AE	0	Hour alarm is enabled.
		1	Hour alarm is disabled.
Alarm: Day		**Address 0B**	
5..0	Alarm days	01 - 31	This register holds the day alarm information coded in BCD format.
7	AE	0	Day alarm is enabled.
		1	Day alarm is disabled.
Alarm: Weekday		**Address 0C**	
2..0	Alarm weekdays	00 - 00	This register holds the weekday alarm information coded in BCD format.
7	AE	0	Weekday alarm is enabled.
		1	Weekday alarm is disabled.
CLKOUT frequency		**Address 0D**	
1..0	FD1, FD0		These bits control the frequency output on the CLKOUT pin, see table 2.
7	FE	0	The CLKOUT output is inhibited and CLKOUT output is set to logic 0.
		1	The CLKOUT output is activated.

BIT NO.	BIT NAME	BIT VALUE	DESCRIPTION
Countdown Timer		**Address 0E and 0F**	
			The timer register is an 8-bit binary countdown timer. It is enabled and disabled via the timer control register bit TE. The source clock for the timer is also selected by the timer control register. Other timer properties such as interrupt generation are controlled via control/status 2 registers. For accurate read back of the countdown value, the I^2C clock (SDA) must be operating at a frequency of at least twice the selected timer clock.
Timer control		**Address 0E**	
1..0	TD1, TD0		Timer source clock frequency select. These bits determine the source clock for the countdown timer, see table 3. When not in use, TD1 & TD0 should be set to 1/60 Hz for power saving.
7	TE	0	Timer is disabled.
		1	Timer is enabled.
Timer countdown value		**Address 0F**	
7..0	Timer	00..FF	Countdown value, n. $\text{CountdownPeriod} = \frac{n}{\text{SourceClockFrequency}}$

Notes

1. The PCF8563 compensates for leap years by adding a 29th day to February if the year counter contains a value which is exactly divisible by 4, including the year 00.
2. These bits may be re-assigned by the user.

Table 1 $\overline{\text{INT}}$ OPERATION (TI/TP=1)

$\overline{\text{INT}}$ PERIOD		
SOURCE CLOCK	**n = 1**	**n > 1**
4096 Hz	1/8192 s	1/4096 s
64 Hz	1/128 s	1/64 s
1 Hz	1/64 s	1/64 s
1/60 Hz	1/64 s	1/64 s

Notes

1. n = Loaded countdown value.
   Timer stopped when n = 0.
2. TF and $\overline{\text{INT}}$ become active simultaneously.

Table 2 FD1, FD0: CLKOUT frequency selection.

FD1	FD0	CLKOUT FREQUENCY
0	0	32.768 kHz
0	1	1024 Hz
1	0	32 Hz
1	1	1 Hz

Table 3 TD1, TD0: Timer frequency selection.

TD1	TD0	TIMER SOURCE CLOCK FREQUENCY
0	0	4096 Hz
0	1	64 Hz
1	0	1 Hz
1	1	1/60 Hz

Table 4 Weekday assignments.

DAY	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Sunday	x	x	x	x	x	0	0	0
Monday	x	x	x	x	x	0	0	1
Tuesday	x	x	x	x	x	0	1	0
Wednesday	x	x	x	x	x	0	1	1
Thursday	x	x	x	x	x	1	0	0
Friday	x	x	x	x	x	1	0	1
Saturday	x	x	x	x	x	1	1	0

Table 5 Month assignments

MONTH	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
January	C	x	x	0	0	0	0	1
February	C	x	x	0	0	0	1	0
March	C	x	x	0	0	0	1	1
April	C	x	x	0	0	1	0	0
May	C	x	x	0	0	1	0	1
June	C	x	x	0	0	1	1	0
July	C	x	x	0	0	1	1	1
August	C	x	x	0	1	0	0	0
September	C	x	x	0	1	0	0	1
October	C	x	x	1	0	0	0	0
November	C	x	x	1	0	0	0	1
December	C	x	x	1	0	0	1	0

EXT_CLK test mode.

A test mode is available which allows for on board testing. In such a mode it is possible to set up test conditions and control the operation of the RTC.

The test mode is entered by setting the TEST1 bit in Control/Status1. The CLKOUT pin then becomes an input. The test mode replaces the internal 64 Hz signal with that applied to the CLKOUT pin. Every 64 positive edges applied to CLKOUT will then generate an increment of one second.

The signal applied to the CLKOUT pin should have a minimum pulse width of 300ns and a minimum period of 1000ns. The internal 64 Hz clock, now sourced from CLKOUT, is divide down to 1 Hz by a 2^6 divide chain called a pre-scaler. The pre-scaler can be set into a known state by using the STOP bit. When the STOP bit is set, the pre-scaler is reset to 0. (STOP must be cleared before the pre-scaler can operate again).

From a STOP condition, the first 1 second increment will take place after 32 positive edges on CLKOUT. Thereafter, every 64 positive edges will cause a 1 second increment.

Note. Entry into EXT_CLK test mode is not synchronized to the internal 64 Hz clock. When entering the test mode, no assumption as to the state of the pre-scaler can be made.

OPERATION EXAMPLE.

1. Set EXT_CLK test mode (Bit7 Control/Status1 = 1).
2. Set STOP (Bit5 Control/Status1 = 1).
3. Clear STOP (Bit5 Control/Status1 = 0).
4. Set time registers to desired value.
5. Apply 32 clock pulses to CLKOUT.
6. Read time registers to see the first change.
7. Apply 64 clock pulses to CLKOUT.
8. Read time registers to see the second change.

Repeat 7 & 8 for additional increments.

Power On Reset override.

The POR duration is directly related to the crystal oscillator start-up time. Due to the long start-up times experienced by these types of circuits, a mechanism has been built in to disable the POR and hence speed up on board test of the device. The setting of this mode requires that the I^2C pins, SDA and SCL, be toggled in a specific order as shown in figure 3. All timings are required minimums.

Once the override mode has been entered, the chip immediately stops being reset and normal operation may commence i.e. entry into the EXT_CLK test mode via I^2C access. The override mode may be cleared by writing a 0 to TESTC. TESTC must be set to 1 before re-entry into the override mode is possible. Setting TESTC to 0 during normal operation has no effect except to prevent entry into the POR override mode.

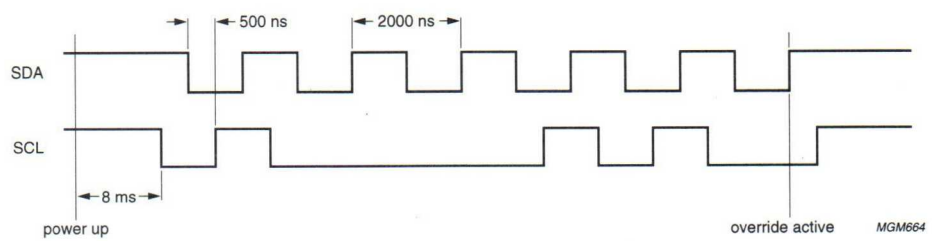


Fig.3 POR override sequence.

LIMITING VALUES.

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+6.5	V
V_I	input voltage	−0.5	V_{DD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
I_{DD}	Supply current	−50	+50	mA
I_{SS}	Supply current	−50	+50	mA
P_{TOT}	total power dissipation	−	300	mW
T_{AMB}	operating ambient temperature	−40	+85	°C
T_{STG}	storage temperature	−65	+150	°C

CHARACTERISTICS OF THE I²C-BUS.

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

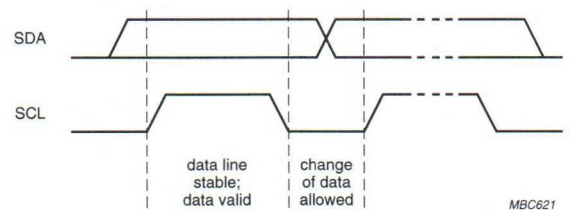


Fig.4 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

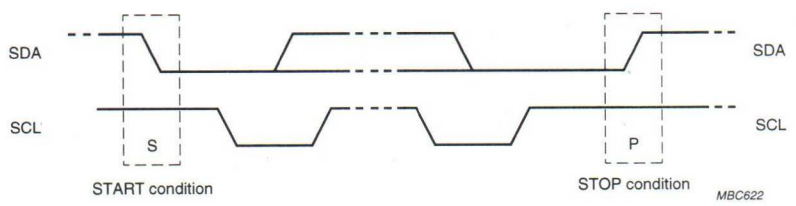


Fig.5 Definition of start and stop conditions.

System configuration (see Fig.6)

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

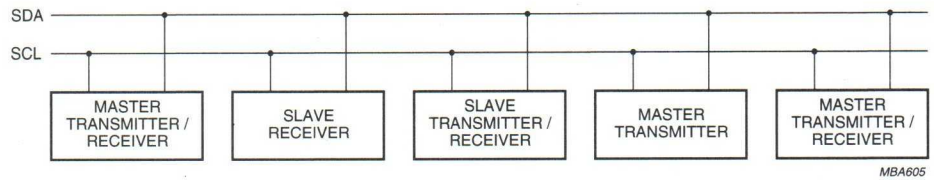


Fig.6 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

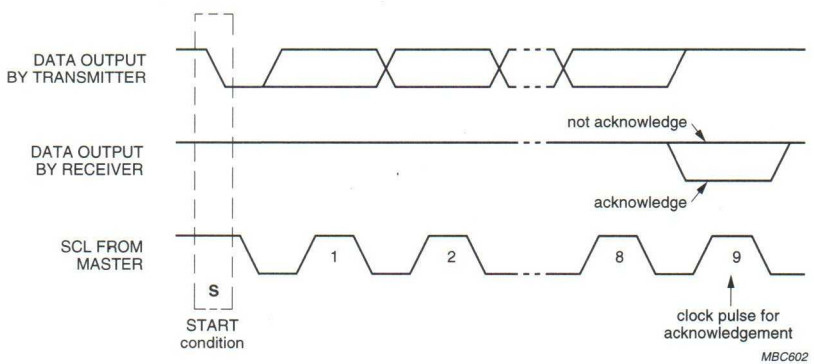


Fig.7 Acknowledgment on the I^2C-bus.

I²C-BUS PROTOCOL.

Addressing

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure.

The PCF8563 acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line.

The PCF8563 slave address is shown in Fig.8.

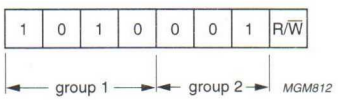


Fig.8 Slave address.

Clock/calendar READ/WRITE cycles

The I²C-bus configuration for the different PCF8563 READ and WRITE cycles is shown below. The word address is four bit value that defines which register is to be accessed next. The upper four bits of the word address are not used.

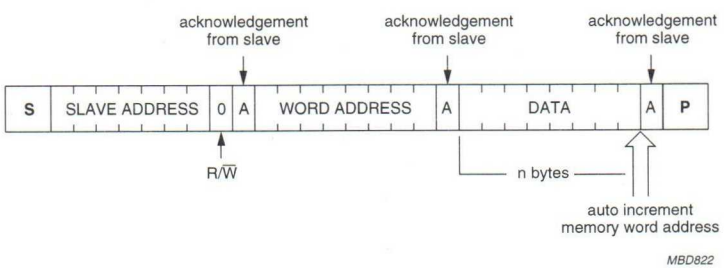


Fig.9 Master transmits to slave receiver (WRITE) mode.

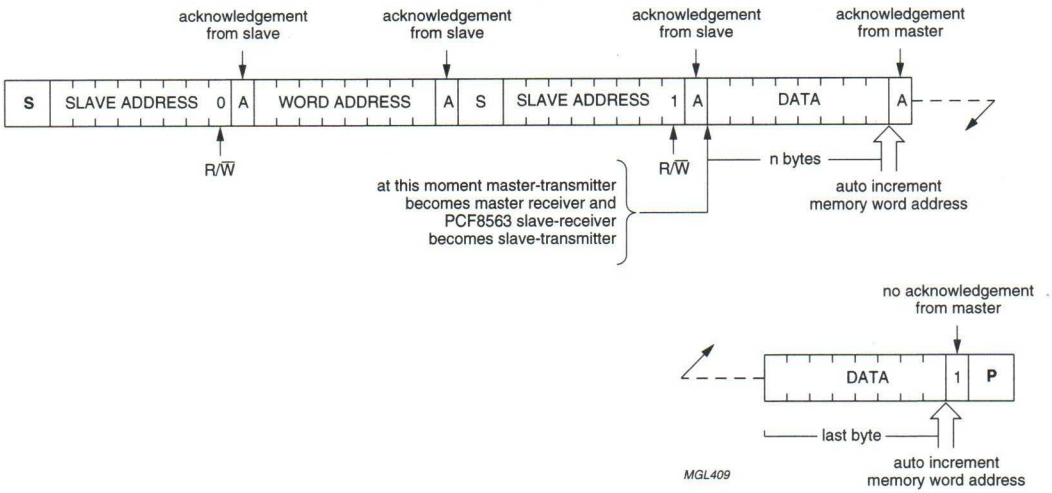


Fig.10 Master reads after setting word address (write word address; READ data).

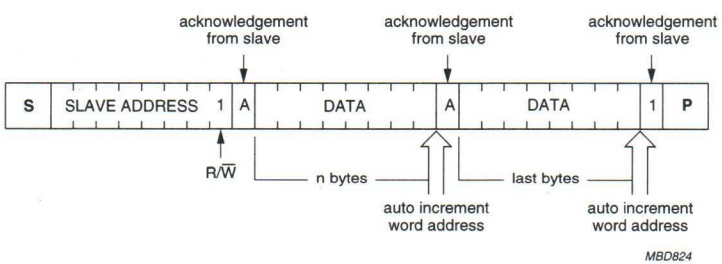


Fig.11 Master reads slave immediately after first byte (READ mode).

DC CHARACTERISTICS.

V_{DD} = 1.8 to 5.5 V; V_{SS} = 0 V; T_{AMB} = −40 to +85 °C; f_{OSC} = 32.768 kHz; quartz R_S = 40 kΩ, C_L = 8 pF unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage (1)	I^2C bus inactive, 25 °C	1.0	–	5.5	V
		400 kHz I^2C bus activity	1.8	–	5.5	V
	clock data integrity	25 °C	V_{LOW}	–	5.5	V
I_{DD}	supply current (2)	f_{SCL} = 400 kHz	–	–	800	μA
		f_{SCL} = 100 kHz	–	–	200	μA
		f_{SCL} = 0 Hz V_{DD} = 5.0 V 25 °C	–	0.3	1.0	μA
		f_{SCL} = 0 Hz V_{DD} = 2.0 V 25 °C	–	0.25	0.75	μA
Inputs						
V_{IL}	LOW level input voltage		V_{SS}	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage	$V_I = V_{DD}$ or V_{SS}	−1	–	1	μA
C_I	input capacitance	(note 3)	–	–	7	pF
Outputs						
$I_{OL(SDA)}$	SDA LOW output current	V_{OL} = 0.4 V, V_{DD} = 5 V	−3	–	–	mA
$I_{OL(\overline{INT})}$	$\overline{INT}$ LOW output current	V_{OL} = 0.4 V, V_{DD} = 5 V	−1	–	–	mA
$I_{OL(CLKOUT)}$	CLKOUT LOW output current	V_{OL} = 0.4 V, V_{DD} = 5 V	−1	–	–	mA
$I_{OH(CLKOUT)}$	CLKOUT HIGH output current	V_{OH} = 4.6 V, V_{DD} = 5 V	1	–	–	mA
I_{LO}	output leakage	$V_O = V_{DD}$ or V_{SS}	−1	–	1	μA
Voltage detector						
V_{LOW}	Low voltage detection	25 °C	–	0.9	1.0	V

Notes

1. When powering up the device, V_{DD} must exceed the specified minimum value by 300 mV to guarantee correct start-up of the oscillator.
2. CLKOUT disabled, (FE = 0). Timer source clock = $1/60$ Hz.
3. Tested on sample basis.

AC CHARACTERISTICS.

V_{DD} = 1.8 to 5.5 V; V_{SS} = 0 V; T_{AMB} = –40 to +85 °C; f_{OSC} = 32.768 kHz; quartz R_S = 40 kΩ, C_L = 8 pF unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator						
C_L	integrated load capacitance		19	25	31	pF
f/f_{OSC}	oscillator stability	for ΔV_{DD} = 200 mV; 25 °C	–	$2x10^{-7}$	–	–
Quartz crystal parameters (f = 32.768 kHz)						
R_s	series resistance		–	–	40	kΩ
C_L	parallel load capacitance		–	10	–	pF
C_T	trimmer capacitance		5	–	25	pF
CLKOUT output						
T_{CLKOUT}	CLKOUT duty cycle	note 1	–	50	–	%
Timing characteristics: I²C-bus; notes 5 & 6						
f_{SCL}	SCL clock frequency	note 4	–	–	400	kHz
$t_{HD;STA}$	START condition hold time		0.6	–	–	µs
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	–	–	µs
t_{LOW}	SCL LOW time		1.3	–	–	µs
t_{HIGH}	SCL HIGH time		0.6	–	–	µs
t_r	SCL and SDA rise time		–	–	0.3	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
C_B	capacitive bus line load		–	–	400	pF
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{SU;STO}$	set-up time for STOP condition		4.0	–	–	µs
t_{SW}	tolerable spike width on bus		–	–	50	ns

Notes

1. Unspecified for f_{CLKOUT} = 32.768 kHz.
2. All timing values are valid within the operating supply voltage at ambient temperature and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
3. A detailed description of the I²C bus specification, with applications, is given in brochure "The I²C bus and how to use it". This brochure may be ordered using the code 9398 393 40011.
4. I²C access time between two STARTs or between a START and a STOP condition to this device must be less than one second.

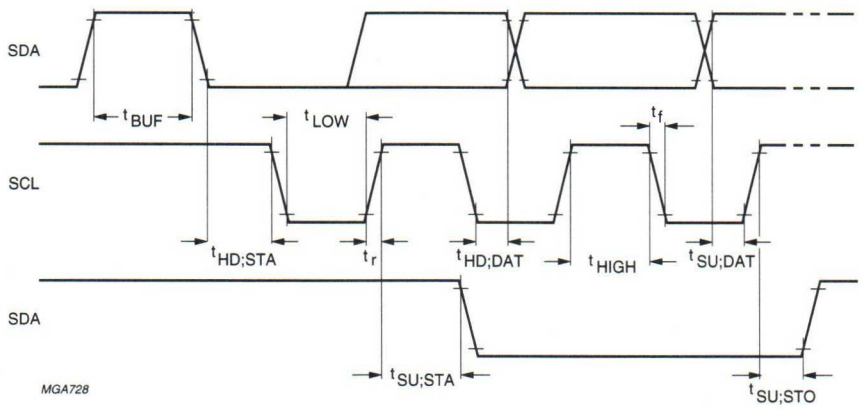


Fig.12 I²C-bus timing waveforms.

APPLICATION INFORMATION

Quartz frequency adjustment

METHOD 1: FIXED OSCI CAPACITOR

By evaluating the average capacitance necessary for the application layout a fixed capacitor can be used. The frequency is best measured via the 32.768 kHz signal available after power-on at the CLKOUT pin. The frequency tolerance depends on the quartz crystal tolerance, the capacitor tolerance and the device-to-device tolerance (on average $\pm 5 \times 10^{-6}$). Average deviations of ±5 minutes per year can be easily achieved.

METHOD 2: OSCI TRIMMER

Using the 32.768 kHz signal available after power-on at the CLKOUT pin fast setting of a trimmer is possible.

METHOD 3:

Direct measurement of OSCO out (accounting for test probe capacitance).

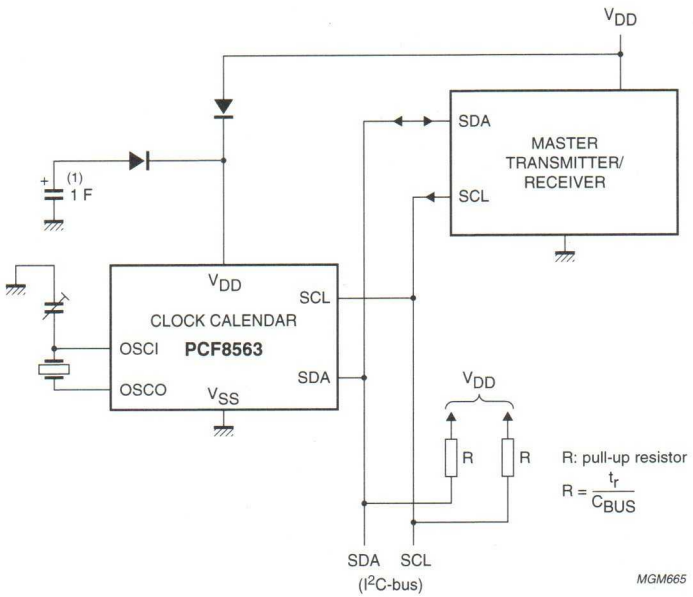


Fig.13 Application diagram.

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Clock/calendar with Power Fail Detector PCF8573

1 FEATURES

- Serial input/output I²C-bus interface for minutes, hours, days and months
- Additional pulse outputs for seconds and minutes
- Alarm register for presetting a time for alarm or remote switching functions
- On-chip power fail detector
- Separate ground pin for the clock allows easy implementation of battery back-up during supply interruption
- Crystal oscillator control (32.768 kHz)
- Low power consumption.

2 GENERAL DESCRIPTION

The PCF8573 is a low threshold, CMOS circuit that functions as a real time clock/calendar. Addresses and data are transferred serially via the two-line bidirectional I²C-bus.

The IC incorporates an addressable time counter and an addressable alarm register for minutes, hours, days and months. Three special control/status flags, COMP, POWF and NODA, are also available. Back-up for the clock during supply interruptions is provided by a 1.2 V nickel cadmium battery. The time base is generated from a 32.768 kHz crystal-controlled oscillator.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{DD} - V_{SS1}$	supply voltage, clock (pin 16 to pin 15)	1.1	–	6.0	V
$V_{DD} - V_{SS2}$	supply voltage, I²C-bus (pin 16 to pin 8)	2.5	–	6.0	V
f_{osc}	crystal oscillator frequency	–	32.768	–	kHz

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8573P	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1
PCF8573T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1

5 BLOCK DIAGRAM

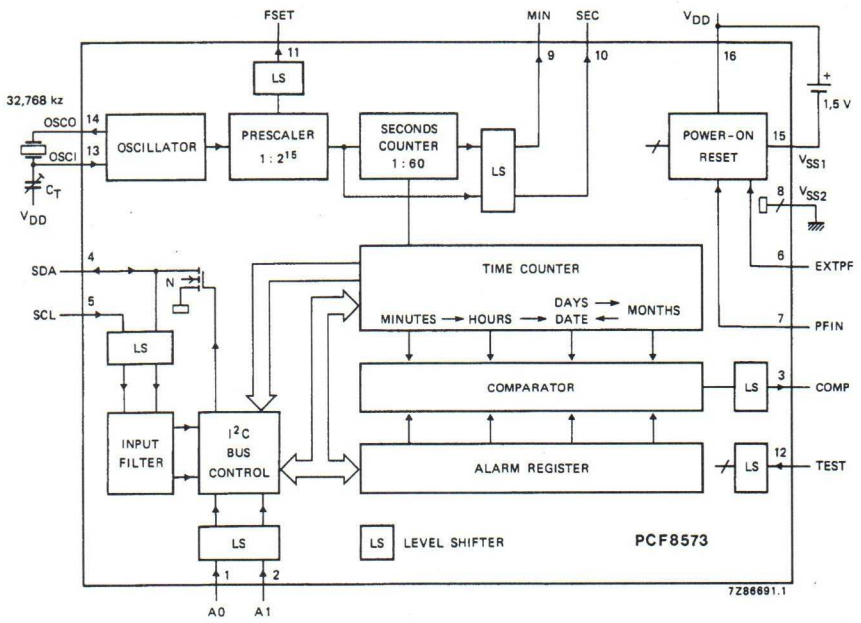


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
A0	1	address input
A1	2	address input
COMP	3	comparator output
SDA	4	serial data line; I^2C-bus
SCL	5	serial clock line; I^2C-bus
EXTPF	6	enable power fail flag input
PFIN	7	power fail flag input
V_{SS2}	8	negative supply 2 (I^2C interface)
MIN	9	one pulse per minute output
SEC	10	one pulse per second output
FSET	11	oscillator tuning output
TEST	12	test input; connect to V_{SS2} if not in use
OSCI	13	oscillator input
OSCO	14	oscillator input/output
V_{SS1}	15	negative supply 1 (clock)
V_{DD}	16	common positive supply

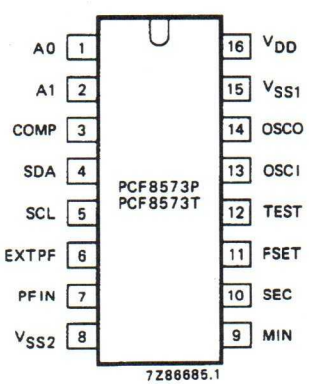


Fig.2 Pinning diagram.

7 FUNCTIONAL DESCRIPTION

7.1 Oscillator

The PCF8573 has an integrated crystal-controlled oscillator which provides the timebase for the prescaler. The frequency is determined by a single 32.76 kHz crystal connected between OSCI and OSCO. A trimmer is connected between OSCI and V_{DD}.

7.2 Prescaler and time counter

The prescaler provides a 128 Hz signal at the FSET output for fine adjustment of the crystal oscillator without loading it. The prescaler also generates a pulse once a second to advance the seconds counter. The carry of the prescaler and the seconds counter are available at the outputs SEC, MIN respectively, and are also readable via the I²C-bus. The mark-to-space ratio of both signals is 1 : 1. The time counter is advanced one count by the falling edge of output signal MIN. A transition from HIGH-to-LOW of output signal SEC triggers MIN to change state. The time counter counts minutes, hours, days and months, and provides a full calendar function which needs to be corrected only once every four years - to allow for leap-year. Cycle lengths are shown in Table 1.

7.3 Alarm register

The alarm register is a 24-bit memory. It stores the time-point for the next setting of the status flag COMP. Details of writing and reading of the alarm register are included in the description of the characteristics of the I²C-bus.

7.4 Comparator

The comparator compares the contents of the alarm register and the time counter, each with a length of 24 bits. When these contents are equal the flag COMP will be set 4 ms after the falling edge of MIN. This set condition occurs once at the beginning of each minute. This information is latched, but can be cleared by an instruction via the I²C-bus. A clear instruction may be transmitted immediately after the flag is set and will be executed. Flag COMP information is also available at the output COMP. The comparison may be based upon hours and minutes only if the internal flag NODA (no date) is set. Flag NODA can be set and cleared by separate instructions via the I²C-bus, but it is undefined until the first set or clear instruction has been received. Both COMP and NODA flags are readable via the I²C-bus.

Table 1 Cycle length of the time counter

UNIT	NUMBER OF BITS	COUNTING CYCLE	CARRY FOR FOLLOWING UNIT	CONTENT OF MONTH COUNTER
minutes	7	00 to 59	59 → 00	
hours	6	00 to 23	23 → 00	
days(1)	6	01 to 28	28 → 01	2 (note 1)
			or 29 → 01	2 (note 1)
		01 to 30	30 → 01	4, 6, 9, 11
		01 to 31	31 → 01	1, 3, 5, 7, 8, 10, 12
months	5	01 to 12	12 → 01	

Note

1. During February of a leap-year the 'Time Counter Days' may be set to 29 by directly writing into it using the 'execute address' function. Leap-years must be tracked by the system software.

7.5 Power on/power fail detection

If the voltage $V_{DD} - V_{SS1}$ falls below a certain value the operation of the clock becomes undefined. Thus a warning signal is required to indicate that faultless operation of the clock is not guaranteed. This information is latched in a flag called POWF (Power Fail) and remains latched after restoration of the correct supply voltage until a write procedure with EXECUTE ADDRESS has been received. The flag POWF can be set by an internally generated power fail level-discriminator signal for application with ($V_{DD} - V_{SS1}$) greater than V_{TH1}, or by an externally generated power fail signal for application with ($V_{DD} - V_{SS1}$) less than V_{TH1}. The external signal must be applied to the input PFIN. The input stage operates with signals of slow rise and fall times. Internally or externally controlled POWF can be selected by input EXTPF as shown in Table 2.

Table 2 Power fail selection

EXTPF(1)	PFIN(1)	FUNCTION
0	0	power fail is sensed internally
0	1	test mode
1	0	power fail is sensed externally
1	1	no power fail sensed

Note

1. 0 = V_{SS1} (LOW); 1 = V_{DD} (HIGH).

The external power fail control operates by absence of the $V_{DD} - V_{SS2}$ supply. Therefore the input levels applied to PFIN and EXTPF must be within the range of V_{DD}–V_{SS1}. A LOW level at PFIN indicates a power fail. POWF is readable via the I^2C-bus. A power-on reset for the I^2C-bus control is generated on-chip when the supply voltage $V_{DD} - V_{SS2}$ is less than V_{TH2}.

7.6 Interface level shifters

The level shifters adjust the 5 V operating voltage ($V_{DD} - V_{SS2}$) of the microcontroller to the internal supply voltage ($V_{DD} - V_{SS1}$) of the clock/calendar. The oscillator and counter are not influenced by the $V_{DD} - V_{SS2}$ supply voltage. If the voltage $V_{DD} - V_{SS2}$ is absent ($V_{DD} = V_{SS2}$) the output signal of the level shifter is HIGH because V_{DD} is the common node of the $V_{DD} - V_{SS2}$ and the $V_{DD} - V_{SS1}$ supplies. Because the level shifters invert the input signals, the internal circuit behaves as if a LOW signal is present on the inputs. FSET, SEC, MIN and COMP are CMOS push-pull output stages. The driving capability of these outputs is lost when the supply voltage $V_{DD} - V_{SS2} = 0$.

8 CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

8.1 Bit transfer (see Fig.3)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

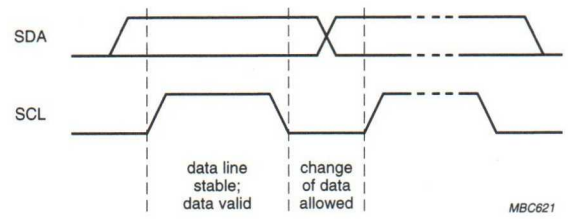


Fig.3 Bit transfer.

8.2 Start and stop conditions (see Fig.4)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

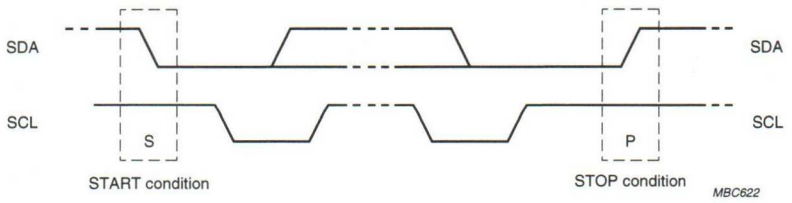


Fig.4 Definition of start and stop conditions.

8.3 System configuration (see Fig.5)

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

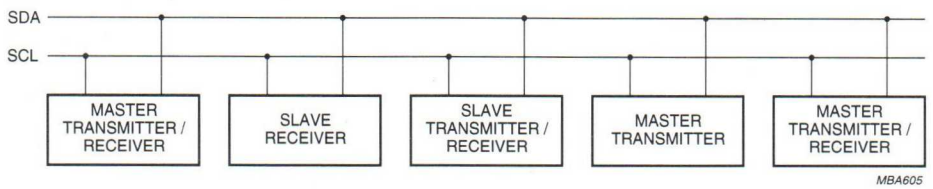


Fig.5 System configuration.

8.4 Acknowledge (see Fig.6)

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the **last byte** that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition, see Figs. 9 and 10.

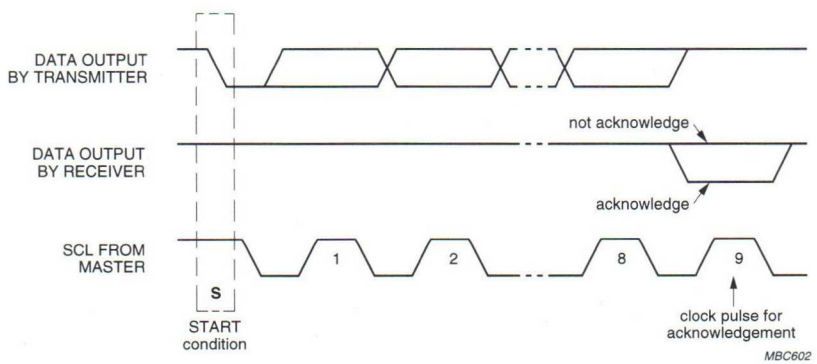


Fig.6 Acknowledgment on the I²C-bus.

9 I²C-BUS PROTOCOL

9.1 Addressing

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

The clock/calendar acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line.

The clock/calendar slave address is shown in Fig.7. Bits A0 and A1 correspond to the two hardware address pins A0 and A1. Connecting these to V_{DD} or V_{SS} allows the device to have 1 of 4 different addresses.

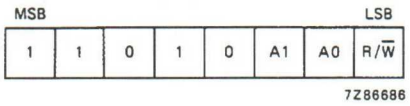


Fig.7 Slave address.

9.2 Clock/calendar READ/WRITE cycles

The I²C-bus configuration for different clock/calendar READ and WRITE cycles is shown in Figs 8, 9 and 10.

The write cycle is used to set the time counter, the alarm register and the flags. The transmission of the clock/calendar address is followed by the MODE-POINTER-word which contains a CONTROL-nibble (Table 3) and an ADDRESS-nibble (Table 4). The ADDRESS-nibble is valid only if the preceding CONTROL-nibble is set to EXECUTE ADDRESS. The third transmitted word contains the data to be written into the time counter or alarm register.

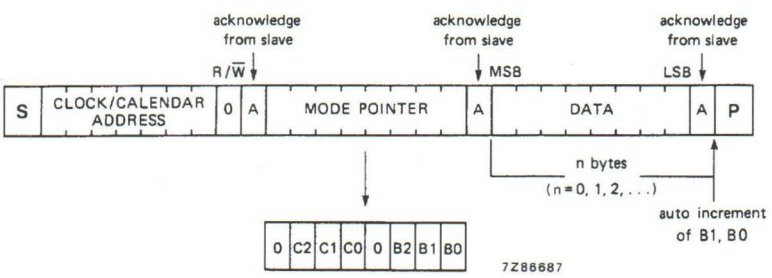
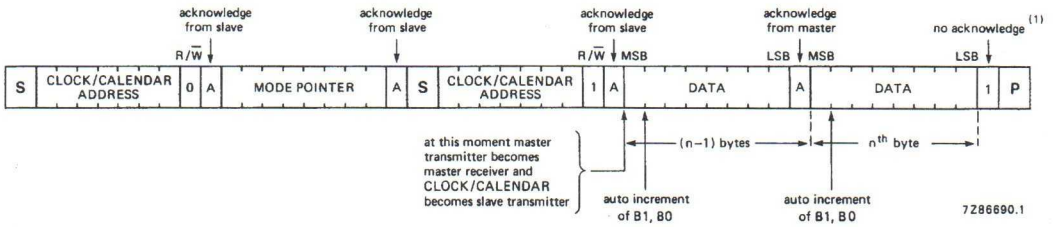
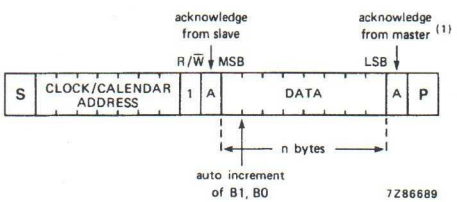


Fig.8 Master transmitter transmits to clock/calendar slave receiver.



(1) The master receiver must signal an end of data to the slave transmitter by **not** generating an acknowledge on the **last byte** that has been clocked out of the slave.

Fig.9 Master transmitter reads clock/calendar after setting mode pointer.



(1) The master receiver must signal an end of data to the slave transmitter by **not** generating an acknowledge on the **last byte** that has been clocked out of the slave.

Fig.10 Master reads clock/calendar immediately after first byte.

Table 3 MODE-POINTER-word, CONTROL-nibble (bits 8, 7, 6 and 5)

BIT 8	C2	C1	C0	FUNCTION
0	0	0	0	execute address
0	0	0	1	read control/status flags
0	0	1	0	reset prescaler, including seconds counter; without carry for minute counter
0	0	1	1	time adjust, with carry for minute counter (note 1)
0	1	0	0	reset NODA flag
0	1	0	1	set NODA flag
0	1	1	0	reset COMP flag

Note

1. If the seconds counter is below 30 there is no carry. This causes a time adjustment of max. –30 s. From the count 30 there is a carry which adjusts the time by max. +30 s.

Table 4 MODE-POINTER-word, ADDRESS-nibble (bits 4, 3, 2 and 1)

BIT 4	B2	B1	B0	ADDRESSED TO:
0	0	0	0	time counter hours
0	0	0	1	time counter minutes
0	0	1	0	time counter days
0	0	1	1	time counter months
0	1	0	0	alarm register hours
0	1	0	1	alarm register minutes
0	1	1	0	alarm register days
0	1	1	1	alarm register months

At the end of each data word the address bits B1, B0 will be incremented automatically provided the preceding CONTROL-nibble is set to EXECUTE ADDRESS. There is no carry to B2.

Table 5 shows the placement of the BCD upper and lower digits in the DATA byte for writing into the addressed part of the time counter and alarm register respectively.

Table 6 shows the acknowledgement response of the clock calendar as a slave receiver.

Table 5 Placement of BCD digits in the DATA byte; note 1

MSB			DATA				LSB	
UPPER DIGIT				LOWER DIGIT				
UD	UC	UB	UA	LD	LC	LB	LA	ADDRESSED TO:
X	X	D	D	D	D	D	D	hours
X	D	D	D	D	D	D	D	minutes
X	X	D	D	D	D	D	D	days
X	X	X	D	D	D	D	D	months

Note

1. 'X' is the don't care bit; 'D' is the data bit.

Acknowledgement response of the PCF8573 as slave-receiver is shown in Table 6. Note that data is only associated with the 'execute address' function where C0, C1, C2 = 0, 0, 0.

Table 6 Slave receiver acknowledgement; note 1

MODE POINTER								ACKNOWLEDGE ON BYTE:		
BIT 8	C2	C1	C0	BIT 4	B2	B1	B0	ADDRESS	MODE POINTER	DATA
0	0	0	0	0	X	X	X	yes	yes	yes
0	0	0	0	1	X	X	X	yes	no	no
0	0	0	1	X	X	X	X	yes	yes	no
0	0	1	0	X	X	X	X	yes	yes	no
0	0	1	1	X	X	X	X	yes	yes	no
0	1	0	0	X	X	X	X	yes	yes	no
0	1	0	1	X	X	X	X	yes	yes	no
0	1	1	0	X	X	X	X	yes	yes	no
0	1	1	1	X	X	X	X	yes	no	no
1	X	X	X	X	X	X	X	yes	no	no

Note

1. 'X' is 'don't care'.

To read the addressed part of the time counter and alarm register, plus information from specified control/status flags, the BCD digits in the DATA byte are organized as shown in Table 7.

The status of the CONTROL-nibble of the MODE-POINTER-WORD (C2, C1, C0) remains unchanged until re-written.

Table 7 Organization of the BCD digits in the DATA byte; note 1

MSB			DATA				LSB	
UPPER DIGIT				LOWER DIGIT				
UD	UC	UB	UA	LD	LC	LB	LA	ADDRESSED TO:
0	0	D	D	D	D	D	D	hours
0	D	D	D	D	D	D	D	minutes
0	0	D	D	D	D	D	D	days
0	0	0	D	D	D	D	D	months
0	0	0	m	s	NODA	COMP	POWF	control/status flags

Note

1. 'D' is the data bit; 'm' = minutes; 's' = seconds.

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_{DD} - V_{SS1}$	supply voltage (pin 16 to pin 15)	−0.3	+8.0	V
$V_{DD} - V_{SS2}$	supply voltage (pin 16 to pin 8)	−0.3	+8.0	V
V_I	input voltage			
	pins 4 and 5 (with input impedance of minimum 500 Ω)	$V_{SS2} - 0.8$	$V_{DD} + 0.8$	V
	pins 6, 7, 13 and 14	$V_{SS1} - 0.6$	$V_{DD} + 0.6$	V
	any other pin	$V_{SS2} - 0.6$	$V_{DD} + 0.6$	V
I_I	DC input current	–	10	mA
I_O	DC output current	–	10	mA
P_{tot}	total power dissipation per package	–	200	mW
P_O	power dissipation per output	–	100	mW
T_{amb}	operating ambient temperature	−40	+85	°C
T_{stg}	storage temperature	−55	+125	°C

11 HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC12 under *"Handling MOS Devices"*.

12 DC CHARACTERISTICS

V_{SS2} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified. Typical values at T_{amb} = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
$V_{DD} - V_{SS2}$	supply voltage (I^2C interface)		2.5	5.0	6.0	V
$V_{DD} - V_{SS1}$	supply voltage (clock)	$t_{HD;DAT} \geq 300$ ns	1.1	1.5	$V_{DD} - V_{SS2}$	V
I_{SS1}	supply current at V_{SS1} (pin 15)	see Fig.11				
		$V_{DD} - V_{SS1}$ = 1.5 V	–	−3	−10	µA
		$V_{DD} - V_{SS1}$ = 5 V	–	−12	−50	µA
I_{SS2}	supply current at V_{SS2} (pin 8)	$V_{DD} - V_{SS2}$ = 5 V; I_O = 0 all outputs	–	–	−50	µA
Input SCL, input/output SDA						
V_{IL}	LOW level input voltage		–	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
I_{LI}	input leakage current	$V_I = V_{SS2}$ or V_{DD}	−1	–	+1	µA
C_i	input capacitance		–	–	7	pF
Inputs A0, A1, TEST						
V_{IL}	LOW level input voltage		–	–	$0.2V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	–	V
I_{LI}	input leakage current	$V_I = V_{SS2}$ or V_{DD}	−250	–	+250	nA
Inputs EXTPF, PFIN						
V_{IL}	LOW level input voltage		0	–	$0.2V_{DD} - V_{SS1}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD} - V_{SS1}$	–	–	V
I_{LI}	input leakage current	$V_I = V_{SS1}$ to V_{DD}	−1.0	–	+1.0	µA
		$V_I = V_{SS1}$ to V_{DD}; T_{amb} = 25 °C	−0.1	–	+0.1	µA
Output SDA (n channel open-drain)						
V_{OL}	LOW level output voltage	output ON; I_O = 3 mA; $V_{DD} - V_{SS2}$ = 2.5 to 6 V	–	–	0.4	V
I_{LI}	input leakage current	$V_{DD} - V_{SS2}$ = 6 V; V_O = 6 V	−1.0	–	+1.0	µA
Output SEC, MIN, COMP, FSET (normal buffer outputs)						
V_{OL}	LOW level output voltage	$V_{DD} - V_{SS2}$ = 2.5 V; I_O = 0.3 mA	–	–	0.4	V
		$V_{DD} - V_{SS2}$ = 4 to 6 V; I_O = 1.6 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	$V_{DD} - V_{SS2}$ = 2.5 V; I_O = −0.1 mA	$V_{DD} - 0.4$	–	–	V
		$V_{DD} - V_{SS2}$ = 4 to 6 V; I_O = −0.5 mA	$V_{DD} - 0.4$	–	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Internal threshold voltages						
V_{TH1}	Power failure detection		1	1.2	1.4	V
V_{TH2}	Power-on reset		1.5	2.0	2.5	V

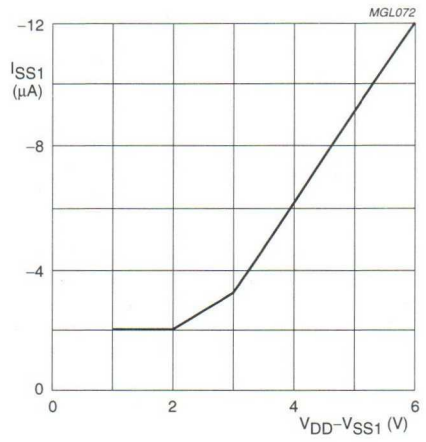


Fig.11 Typical supply current (I_{SS1}) as a function of clock supply voltage ($V_{DD} - V_{SS1}$) at T_{amb} = −40 to +85 °C.

13 AC CHARACTERISTICS

V_{SS2} = 0 V; T_{amb} = −40 to +85 °C unless otherwise specified. Typical values at T_{amb} = +25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Rise and fall times of input signals						
t_r	rise time	input EXTPF	–	–	1	µs
		input PFIN	–	–	∞	µs
		all other inputs (levels between V_{IL} and V_{IH})	–	–	1	µs
t_f	fall time	input EXTPF	–	–	1	µs
		input PFIN	–	–	∞	µs
		all other inputs (levels between V_{IL} and V_{IH})	–	–	0.3	µs
Oscillator						
C_{osc}	integrated oscillator capacitance		–	40	–	pF
R_f	oscillator feedback resistance		–	3	–	MΩ
Δf_{osc}	oscillator stability	$\Delta(V_{DD} - V_{SS1})$ = 100 mV; T_{amb} = 25 °C; $(V_{DD} - V_{SS1})$ = 1.55 V	–	2×10^{-7}	–	
Quartz crystal parameters (f = 32.768 kHz)						
R_s	series resistance		–	–	40	kΩ
C_L	parallel load capacitance		–	10	–	pF
C_T	trimmer capacitance		5	–	25	pF
I²C-bus timing (see Fig.12; notes 1 and 2)						
f_{SCL}	SCL clock frequency		–	–	100	kHz
t_{SP}	tolerable spike width on bus		–	–	100	ns
t_{BUF}	bus free time		4.7	–	–	µs
$t_{SU;STA}$	START condition set-up time		4.7	–	–	µs
$t_{HD;STA}$	START condition hold time		4.0	–	–	µs
t_{LOW}	SCL LOW time		4.7	–	–	µs
t_{HIGH}	SCL HIGH time		4.0	–	–	µs
t_r	SCL and SDA rise time		–	–	1.0	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{VD;DAT}$	SCL LOW to data out valid		–	–	3.4	µs
$t_{SU;STO}$	STOP condition set-up time		4.0	–	–	µs

Notes

1. All timing values are valid within the operating supply voltage and ambient temperature range and reference to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
2. A detailed description of the I²C-bus specification, with applications, is given in brochure *"The I²C-bus and how to use it"*. This brochure may be ordered using the code 9398 393 40011.

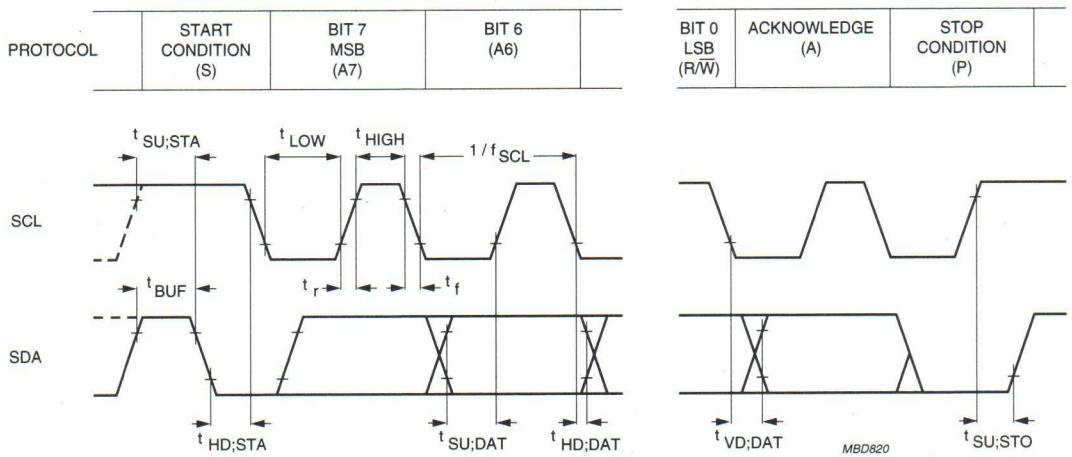


Fig.12 I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

14 APPLICATION INFORMATION

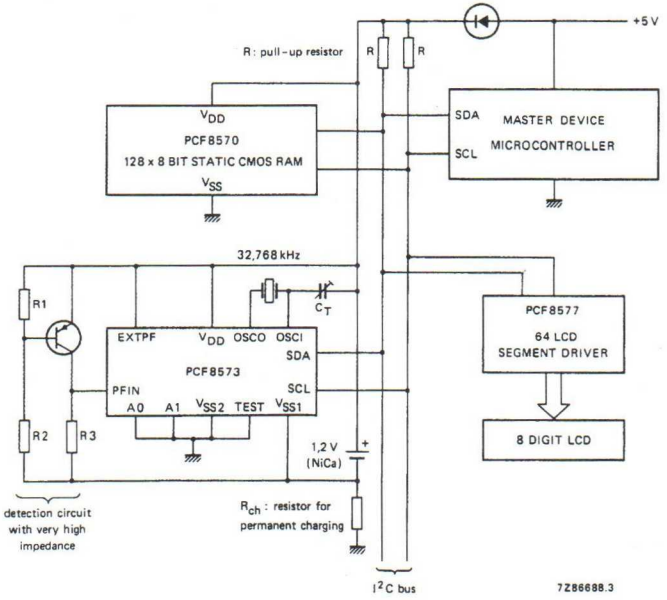


Fig.13 Application example of the PCF8573 clock/calendar with battery backup.

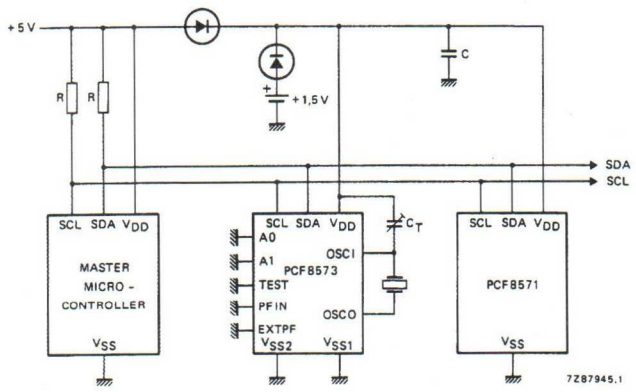


Fig.14 Application example of the PCF8573 with common V_{SS1} and V_{SS2} supply.

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Clock/calendar with 240 × 8-bit RAM PCF8583

1 FEATURES

- I²C-bus interface operating supply voltage: 2.5 V to 6 V
- Clock operating supply voltage (0 to +70 °C): 1.0 V to 6.0 V
- 240 × 8-bit low-voltage RAM
- Data retention voltage: 1.0 V to 6 V
- Operating current (at f_{SCL} = 0 Hz): max. 50 μA
- Clock function with four year calendar
- Universal timer with alarm and overflow indication
- 24 or 12 hour format
- 32.768 kHz or 50 Hz time base
- Serial input/output bus (I²C)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function
- Slave address:
  - READ: A1 or A3
  - WRITE: A0 or A2.

2 GENERAL DESCRIPTION

The PCF8583 is a clock/calendar circuit based on a 2048-bit static CMOS RAM organized as 256 words by 8 bits. Addresses and data are transferred serially via the two-line bidirectional I²C-bus. The built-in word address register is incremented automatically after each written or read data byte. Address pin A0 is used for programming the hardware address, allowing the connection of two devices to the bus without additional hardware.

The built-in 32.768 kHz oscillator circuit and the first 8 bytes of the RAM are used for the clock/calendar and counter functions. The next 8 bytes may be programmed as alarm registers or used as free RAM space. The remaining 240 bytes are free RAM locations.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage operating mode	I²C-bus active	2.5	–	6.0	V
		I²C-bus inactive	1.0	–	6.0	V
I_{DD}	supply current operating mode	f_{SCL} = 100 kHz	–	–	200	μA
I_{DDO}	supply current clock mode	f_{SCL} = 0 Hz; V_{DD} = 5 V	–	10	50	μA
		f_{SCL} = 0 Hz; V_{DD} = 1 V	–	2	10	μA
T_{amb}	operating ambient temperature range		−40	–	+85	°C
T_{stg}	storage temperature range		−65	–	+150	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8583P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCF8583T	SO8	plastic small outline package; 8 leads; body width 7.5 mm	SOT176-1

5 BLOCK DIAGRAM

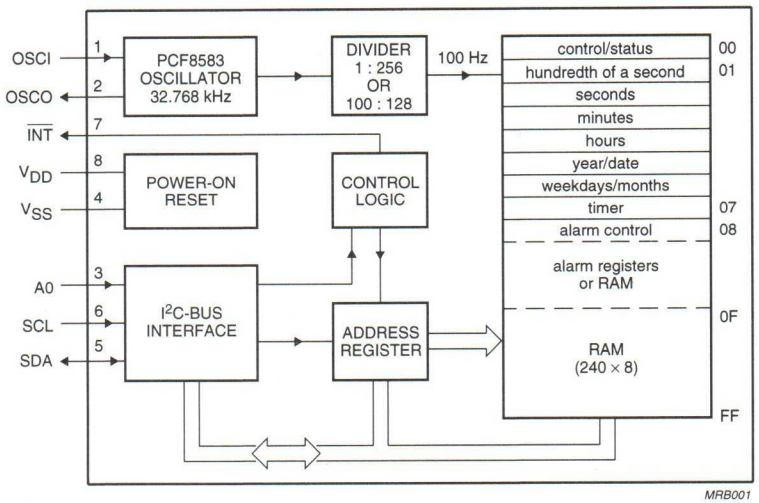


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
OSCI	1	oscillator input, 50 Hz or event-pulse input
OSCO	2	oscillator output
A0	3	address input
V_{SS}	4	negative supply
SDA	5	serial data line
SCL	6	serial clock line
$\overline{INT}$	7	open drain interrupt output (active LOW)
V_{DD}	8	positive supply

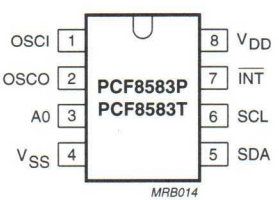


Fig.2 Pinning diagram.

7 FUNCTIONAL DESCRIPTION

The PCF8583 contains a 256 by 8-bit RAM with an 8-bit auto-increment address register, an on-chip 32.768 kHz oscillator circuit, a frequency divider, a serial two-line bidirectional I^2C-bus interface and a power-on reset circuit.

The first 16 bytes of the RAM (memory addresses 00 to 0F) are designed as addressable 8-bit parallel special function registers. The first register (memory address 00) is used as a control/status register. The memory addresses 01 to 07 are used as counters for the clock function. The memory addresses 08 to 0F may be programmed as alarm registers or used as free RAM locations, when the alarm is disabled.

7.1 Counter function modes

When the control/status register is programmed, a 32.768 kHz clock mode, a 50 Hz clock mode or an event-counter mode can be selected.

In the clock modes the hundredths of a second, seconds, minutes, hours, date, month (four year calendar) and weekday are stored in a BCD format. The timer register stores up to 99 days. The event counter mode is used to count pulses applied to the oscillator input (OSCO left open-circuit). The event counter stores up to 6 digits of data.

When one of the counters is read (memory locations 01 to 07), the contents of all counters are strobed into capture latches at the beginning of a read cycle. Therefore, faulty reading of the count during a carry condition is prevented.

When a counter is written, other counters are not affected.

7.2 Alarm function modes

By setting the alarm enable bit of the control/status register the alarm control register (address 08) is activated.

By setting the alarm control register a dated alarm, a daily alarm, a weekday alarm or a timer alarm may be programmed. In the clock modes, the timer register (address 07) may be programmed to count hundredths of a second, seconds, minutes, hours or days. Days are counted when an alarm is not programmed.

Whenever an alarm event occurs the alarm flag of the control/status register is set. A timer alarm event will set the alarm flag and an overflow condition of the timer will set the timer flag. The open drain interrupt output is switched on (active LOW) when the alarm or timer flag is set (enabled). The flags remain set until directly reset by a write operation.

When the alarm is disabled (Bit 2 of control/status register = 0) the alarm registers at addresses 08 to 0F may be used as free RAM.

7.3 Control/status register

The control/status register is defined as the memory location 00 with free access for reading and writing via the I^2C-bus. All functions and options are controlled by the contents of the control/status register (see Fig.3).

7.4 Counter registers

In the clock modes 24 h or 12 h format can be selected by setting the most significant bit of the hours counter register. The format of the hours counter is shown in Fig.5.

The year and date are packed into memory location 05 (see Fig.6). The weekdays and months are packed into memory location 06 (see Fig.7). When reading these memory locations the year and weekdays are masked out when the mask flag of the control/status register is set. This allows the user to read the date and month count directly.

In the event-counter mode events are stored in BCD format. D5 is the most significant and D0 the least significant digit. The divider is by-passed.

In the different modes the counter registers are programmed and arranged as shown in Fig.4. Counter cycles are listed in Table 1.

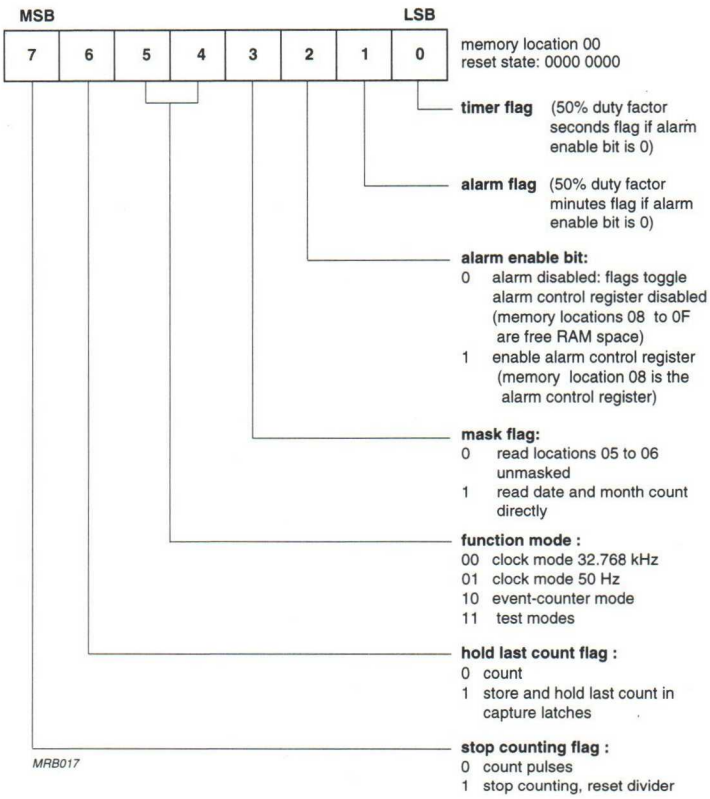


Fig.3 Control/status register.

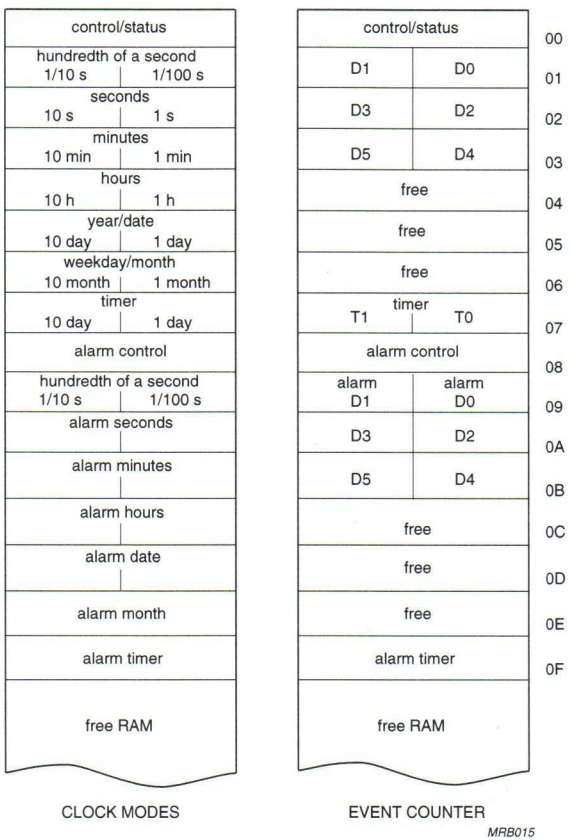


Fig.4 Register arrangement.

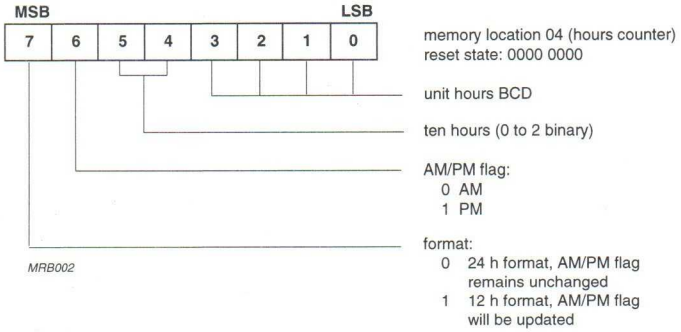


Fig.5 Format of the hours counter.

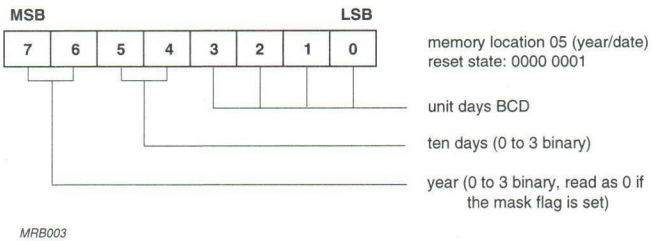


Fig.6 Format of the year/date counter.

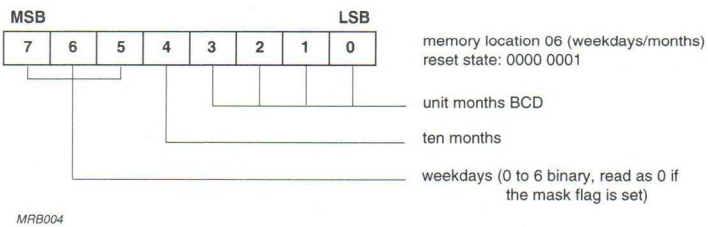


Fig.7 Format of the weekdays/month counter.

Table 1 Cycle length of the time counters, clock modes

UNIT	COUNTING CYCLE	CARRY TO NEXT UNIT	CONTENTS OF THE MONTH COUNTER
Hundredths of a second	00 to 99	99 to 00	–
Seconds	00 to 59	59 to 00	–
Minutes	00 to 59	59 to 00	–
Hours (24 h)	00 to 23	23 to 00	–
Hours (12 h)	12 AM	–	–
	01 AM to 11 AM	–	–
	12 PM	–	–
	01 PM to 11 PM	11 PM to 12 AM	–
Date	01 to 31	31 to 01	1, 3, 5, 7, 8, 10 and 12
	01 to 30	30 to 01	4, 6, 9 and 11
	01 to 29	29 to 01	2, year = 0
	01 to 28	28 to 01	2, year = 1, 2 and 3
Months	01 to 12	12 to 01	–
Year	0 to 3	–	–
Weekdays	0 to 6	6 to 0	–
Timer	00 to 99	no carry	–

7.5 Alarm control register

When the alarm enable bit of the control/status register is set (address 00, bit 2) the alarm control register (address 08) is activated. All alarm, timer, and interrupt output functions are controlled by the contents of the alarm control register (see Fig.8).

7.6 Alarm registers

All alarm registers are allocated with a constant address offset of hexadecimal 08 to the corresponding counter registers (see Fig.4, Register arrangement).

An alarm signal is generated when the contents of the alarm registers matches bit-by-bit the contents of the involved counter registers. The year and weekday bits are ignored in a dated alarm. A daily alarm ignores the month and date bits. When a weekday alarm is selected, the contents of the alarm weekday/month register will select the weekdays on which an alarm is activated (see Fig.9).

Remark: In the 12 h mode, bits 6 and 7 of the alarm hours register must be the same as the hours counter.

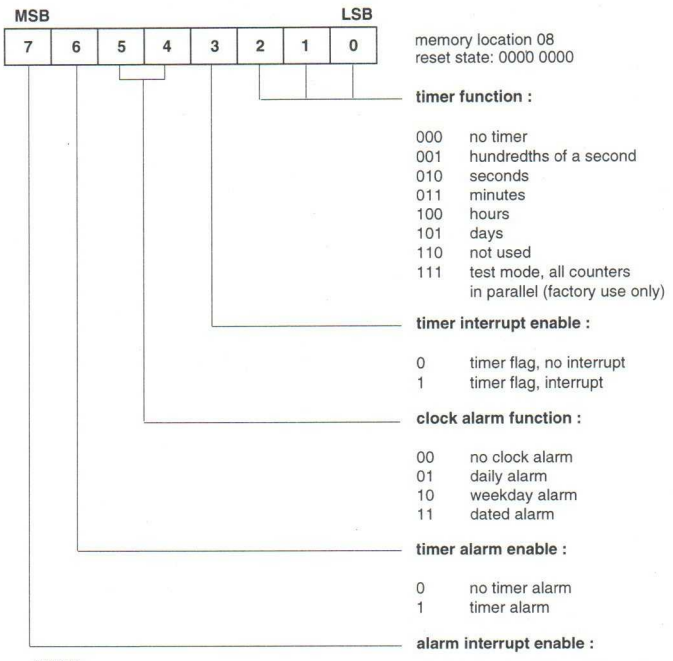


Fig.8 Alarm control register; clock mode.

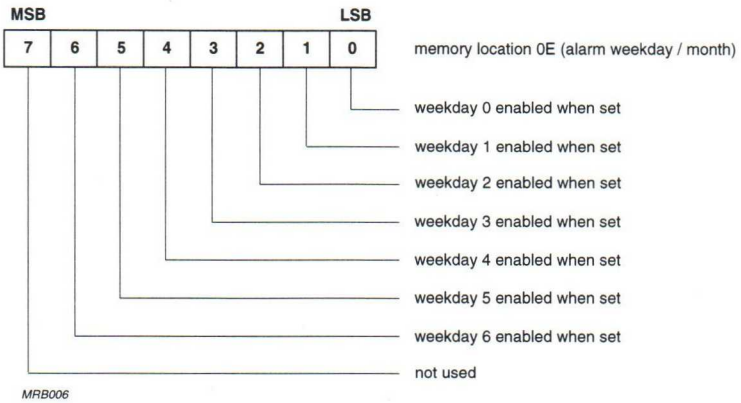


Fig.9 Selection of alarm weekdays.

7.7 Timer

The timer (location 07) is enabled by setting the control/status register = XX0X X1XX. The timer counts up from 0 (or a programmed value) to 99. On overflow, the timer resets to 0. The timer flag (LSB of control/status register) is set on overflow of the timer. This flag must be reset by software. The inverted value of this flag can be transferred to the external interrupt by setting bit 3 of the alarm control register.

Additionally, a timer alarm can be programmed by setting the timer alarm enable (bit 6 of the alarm control register). When the value of the timer equals a pre-programmed value in the alarm timer register (location 0F), the alarm flag is set (bit 1 of the control/status register). The inverted value of the alarm flag can be transferred to the external interrupt by enabling the alarm interrupt (bit 6 of the alarm control register).

Resolution of the timer is programmed via the 3 LSBs of the alarm control register (see Fig.11, Alarm and timer Interrupt logic diagram).

7.8 Event counter mode

Event counter mode is selected by bits 4 and 5 which are logic 1, 0 in the control/status register. The event counter mode is used to count pulses externally applied to the oscillator input (OSCO left open-circuit).

The event counter stores up to 6 digits of data, which are stored as 6 hexadecimal values located in locations 1, 2, and 3. Thus, up to 1 million events may be recorded.

An event counter alarm occurs when the event counter registers match the value programmed in locations 9, A, and B, and the event alarm is enabled (bits 4 and 5 which are logic 0, 1 in the alarm control register). In this event, the alarm flag (bit 1 of the control/status register) is set. The inverted value of this flag can be transferred to the interrupt pin (pin 7) by setting the alarm interrupt enable in the alarm control register. In this mode, the timer (location 07) increments once for every one, one-hundred, ten thousand, or 1 million events, depending on the value programmed in bits 0, 1 and 2 of the alarm control register. In all other events, the timer functions are as in the clock mode.

7.9 Interrupt output

The conditions for activating the open-drain n-channel interrupt output $\overline{\text{INT}}$ (active LOW) are determined by appropriate programming of the alarm control register. These conditions are clock alarm, timer alarm, timer overflow, and event counter alarm. An interrupt occurs when the alarm flag or the timer flag is set, and the corresponding interrupt is enabled. In all events, the interrupt is cleared only by software resetting of the flag which initiated the interrupt.

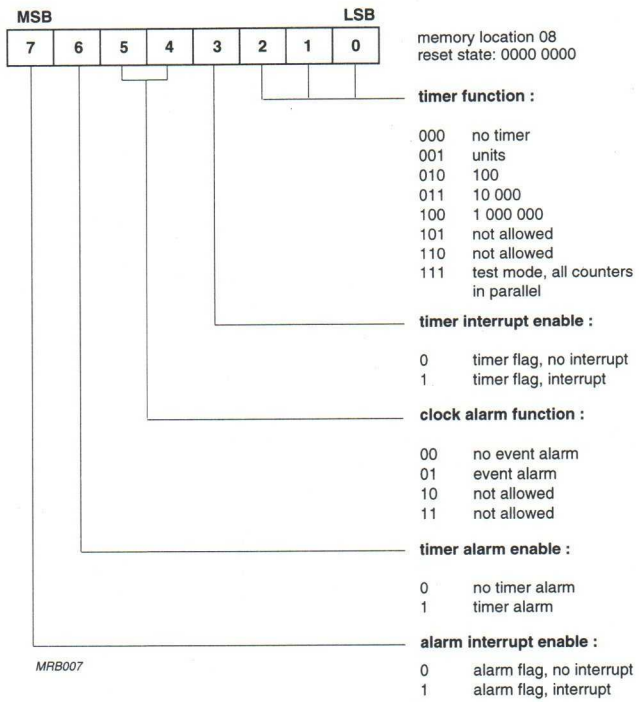


Fig.10 Alarm control register, event-counter mode.

In the clock mode, if the alarm enable is not activated (alarm enable bit of control/status register is logic 0), the interrupt output toggles at 1 Hz with a 50% duty cycle (may be used for calibration). This is the default power-on state of the device. The OFF voltage of the interrupt output may exceed the supply voltage, up to a maximum of 6.0 V. A logic diagram of the interrupt output is shown in Fig.11.

7.10 Oscillator and divider

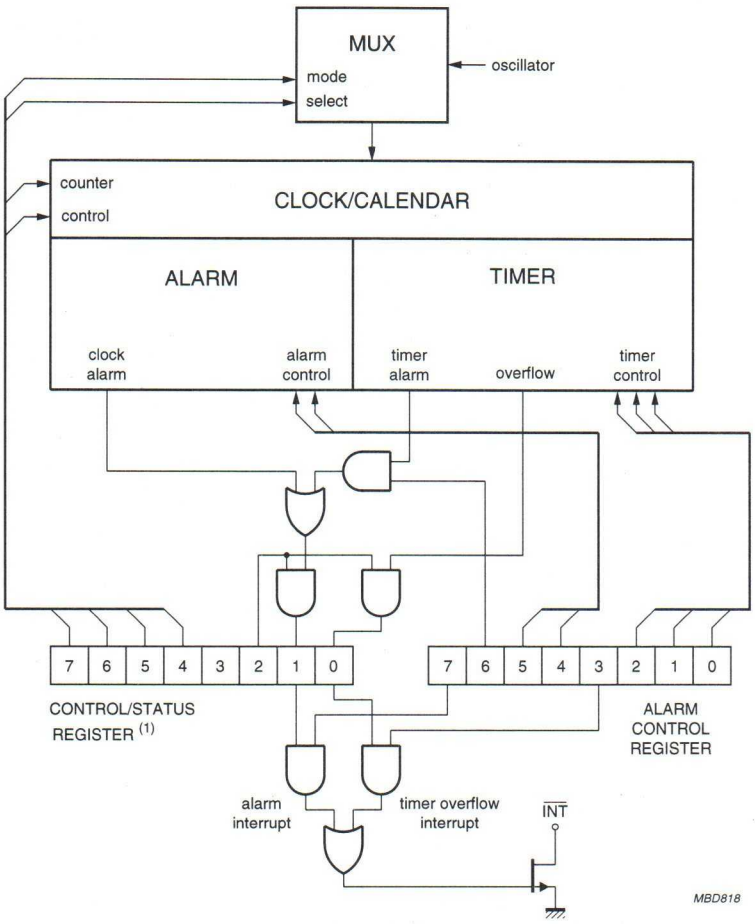
A 32.768 kHz quartz crystal has to be connected to OSCI (pin 1) and OSCO (pin 2). A trimmer capacitor between OSCI and V_{DD} is used for tuning the oscillator (see quartz frequency adjustment). A 100 Hz clock signal is derived from the quartz oscillator for the clock counters.

In the 50 Hz clock mode or event-counter mode the oscillator is disabled and the oscillator input is switched to a high impedance state. This allows the user to feed the 50 Hz reference frequency or an external high speed event signal into the input OSCI.

7.11 Initialization

When power-up occurs the I^2C-bus interface, the control/status register and all clock counters are reset. The device starts time-keeping in the 32.768 kHz clock mode with the 24 h format on the first of January at 0.00.00: 00. A 1 Hz square wave with 50% duty cycle appears at the interrupt output pin (starts HIGH).

It is recommended to set the stop counting flag of the control/status register before loading the actual time into the counters. Loading of illegal states may lead to a temporary clock malfunction.



(1) If the alarm enable bit of the control/status register is reset (logic 0), a 1 Hz signal can be observed on the interrupt pin $\overline{INT}$.

Fig.11 Alarm and timer interrupt logic diagram.

8 CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

8.1 Bit transfer (see Fig.12)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

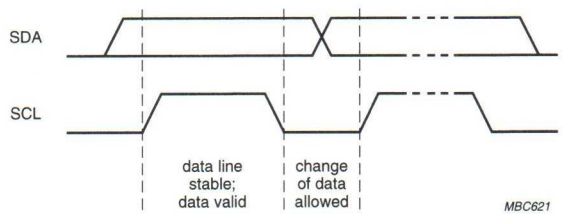


Fig.12 Bit transfer.

8.2 Start and stop conditions (see Fig.13)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

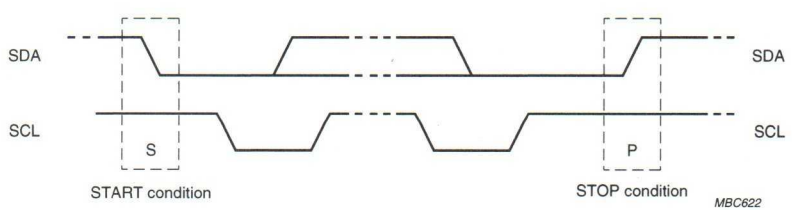


Fig.13 Definition of start and stop conditions.

8.3 System configuration (see Fig.14)

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

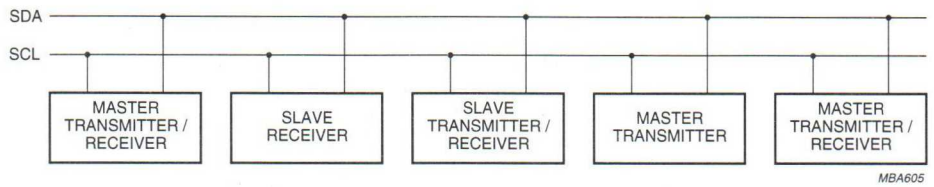


Fig.14 System configuration.

8.4 Acknowledge (see Fig.15)

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

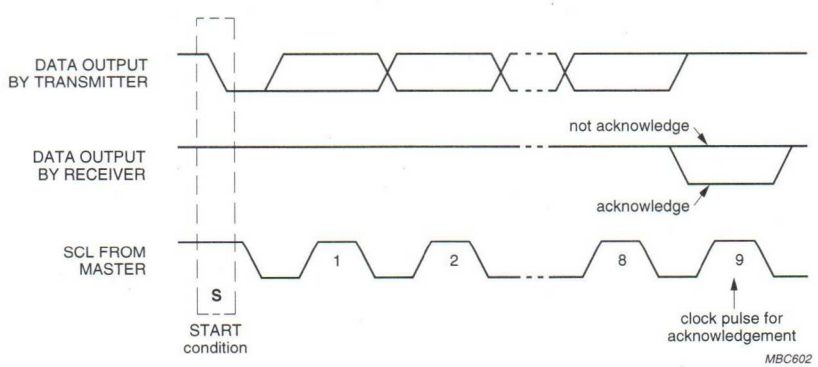


Fig.15 Acknowledgment on the I²C-bus.

9 I²C-BUS PROTOCOL

9.1 Addressing

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure.

The clock/calendar acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line.

The clock/calendar slave address is shown in Fig.16. Bit A0 corresponds to hardware address pin A0. Connecting this pin to V_{DD} or V_{SS} allows the device to have one of two different addresses.

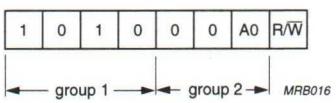


Fig.16 Slave address.

9.2 Clock/calendar READ/WRITE cycles

The I²C-bus configuration for the different PCF8583 READ and WRITE cycles is shown in Figs 17, 18 and 19.

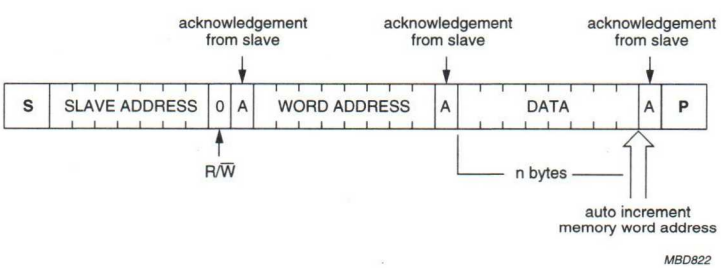


Fig.17 Master transmits to slave receiver (WRITE) mode.

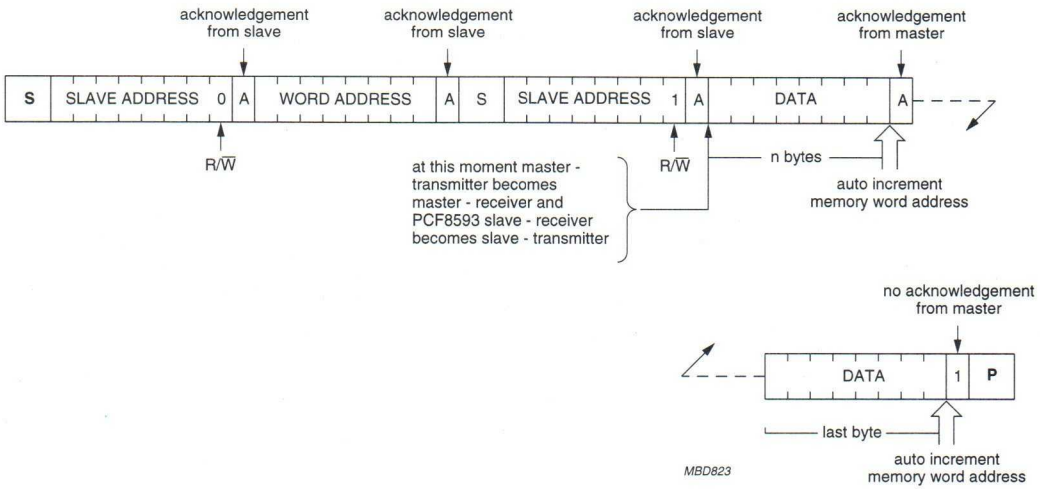


Fig.18 Master reads after setting word address (write word address; READ data).

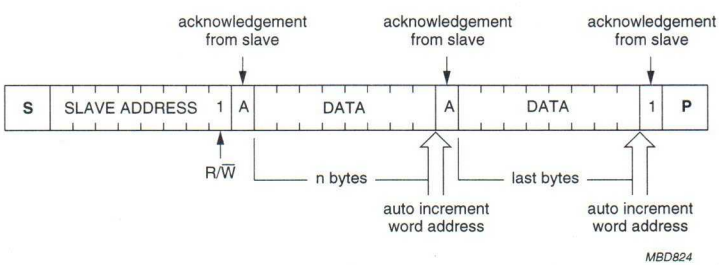


Fig.19 Master reads slave immediately after first byte (READ mode).

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pin 8)	−0.8	+7.0	V
I_{DD}	supply current (pin 8)	–	50	mA
I_{SS}	supply current (pin 4)	–	50	mA
V_I	input voltage	−0.8	V_{DD} + 0.8	V
I_I	DC input current	–	10	mA
I_O	DC output current	–	10	mA
P_{tot}	total power dissipation per package	–	300	mW
P_O	power dissipation per output	–	50	mW
T_{amb}	operating ambient temperature	−40	+85	°C
T_{stg}	storage temperature	−65	+150	°C

11 HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC12 under *"Handling MOS Devices"*.

12 DC CHARACTERISTICS

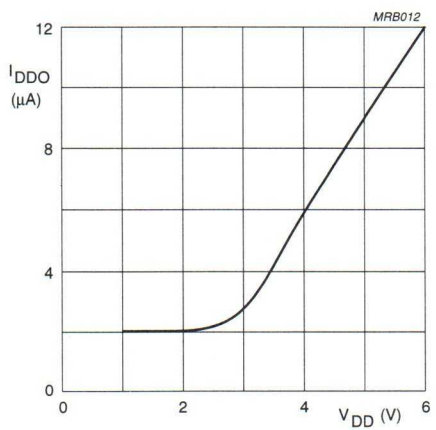
V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
V_{DD}	supply voltage (operating mode)	I^2C-bus active	2.5	–	6.0	V
		I^2C-bus inactive	1.0	–	6.0	V
V_{DDosc}	supply voltage (quartz oscillator)	T_{amb} = 0 to 70 °C; note 2	1.0	–	6.0	V
I_{DD}	supply current (operating mode)	f_{SCL} = 100 kHz; clock mode; note 3	–	–	200	µA
I_{DDO}	supply current (clock mode)	see Fig.20				
		f_{SCL} = 0 Hz; V_{DD} = 5 V	–	10	50	µA
		f_{SCL} = 0 Hz; V_{DD} = 1 V	–	2	10	µA
I_{DDR}	data retention	f_{OSCI} = 0 Hz; V_{DD} = 1 V				
		T_{amb} = −40 to + 85 °C	–	–	5	µA
		T_{amb} = −25 to + 70 °C	–	–	2	µA
V_{EN}	I^2C-bus enable level	note 4	1.5	1.9	2.3	V
SDA						
V_{IL}	LOW level input voltage	note 5	−0.8	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage	note 5	$0.7V_{DD}$	–	V_{DD} +0.8	V
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	–	–	mA
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	µA
C_i	input capacitance	note 6	–	–	7	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
A0; OSCI						
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	−250	–	+250	nA
$\overline{INT}$						
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	–	–	mA
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	µA
SCL						
C_i	input capacitance	note 6	–	–	7	pF
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	µA

Notes

1. Typical values measured at T_{amb} = 25 °C.
2. When powering-up the device, V_{DD} must exceed 1.5 V until stable operation of the oscillator is established.
3. Event counter mode: supply current dependant upon input frequency.
4. The I^2C-bus logic is disabled if $V_{DD} < V_{EN}$.
5. When the voltages are above or below the supply voltages V_{DD} or V_{SS}, an input current may flow; this current must not exceed ±0.5 mA.
6. Tested on sample basis.



f_{SCL} = 32 kHz; T_{amb} = 25 °C.

Fig.20 Typical supply current in clock mode as a function of supply voltage.

13 AC CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator						
C_{osc}	integrated oscillator capacitance		–	40	–	pF
Δf_{osc}	oscillator stability	for ΔV_{DD} = 100 mV; T_{amb} = 25 °C; V_{DD} = 1.5 V	–	2×10^{-7}	–	
f_i	input frequency	note 1	–	–	1	MHz
Quartz crystal parameters (f = 32.768 kHz)						
R_s	series resistance		–	–	40	kΩ
C_L	parallel load capacitance		–	10	–	pF
C_T	trimmer capacitance		5	–	25	pF
I²C-bus timing (see Fig.21; notes 2 and 3)						
f_{SCL}	SCL clock frequency		–	–	100	kHz
t_{SP}	tolerable spike width on bus		–	–	100	ns
t_{BUF}	bus free time		4.7	–	–	µs
$t_{SU;STA}$	START condition set-up time		4.7	–	–	µs
$t_{HD;STA}$	START condition hold time		4.0	–	–	µs
t_{LOW}	SCL LOW time		4.7	–	–	µs
t_{HIGH}	SCL HIGH time		4.0	–	–	µs
t_r	SCL and SDA rise time		–	–	1.0	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{VD;DAT}$	SCL LOW to data out valid		–	–	3.4	µs
$t_{SU;STO}$	STOP condition set-up time		4.0	–	–	µs

Notes

1. Event counter mode only.
2. All timing values are valid within the operating supply voltage and ambient temperature range and reference to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
3. A detailed description of the I²C-bus specification, with applications, is given in brochure *"The I²C-bus and how to use it"*. This brochure may be ordered using the code 9398 393 40011.

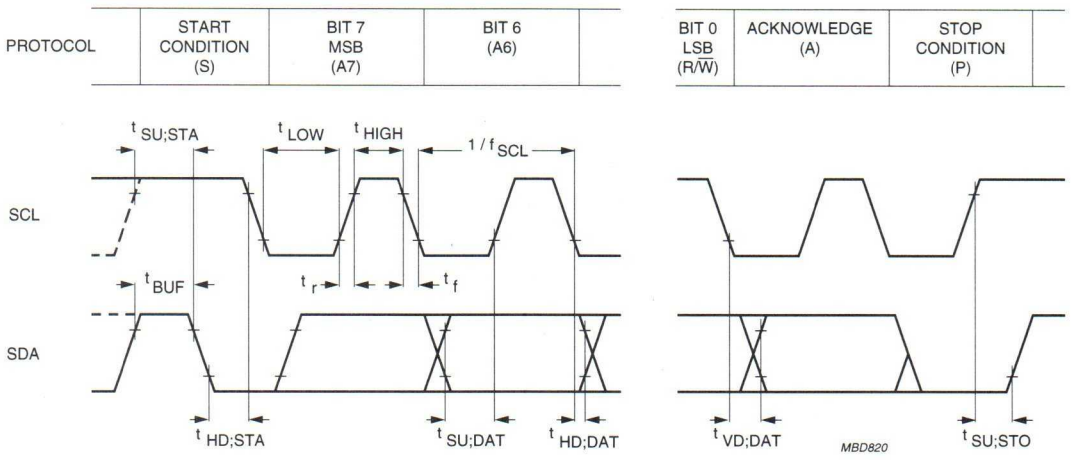


Fig.21 I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

14 APPLICATION INFORMATION

14.1 Quartz frequency adjustment

14.1.1 METHOD 1: FIXED OSCI CAPACITOR

By evaluating the average capacitance necessary for the application layout a fixed capacitor can be used. The frequency is best measured via the 1 Hz signal available after power-on at the interrupt output (pin 7). The frequency tolerance depends on the quartz crystal tolerance, the capacitor tolerance and the device-to-device tolerance (on average $\pm 5 \times 10^{-6}$). Average deviations of ±5 minutes per year can be achieved.

14.1.2 METHOD 2: OSCI TRIMMER

Using the alarm function (via the I²C-bus) a signal faster than 1 Hz can be generated at the interrupt output for fast setting of a trimmer.

Procedure:

- Power-on
- Initialization (alarm functions).

Routine:

- Set clock to time T and set alarm to time T + dT
- At time T + dT (interrupt) repeat routine.

14.1.3 METHOD 3:

Direct measurement of OSC out (accounting for test probe capacitance).

The PCF8583 slave address has a fixed combination 1010 as group 1.

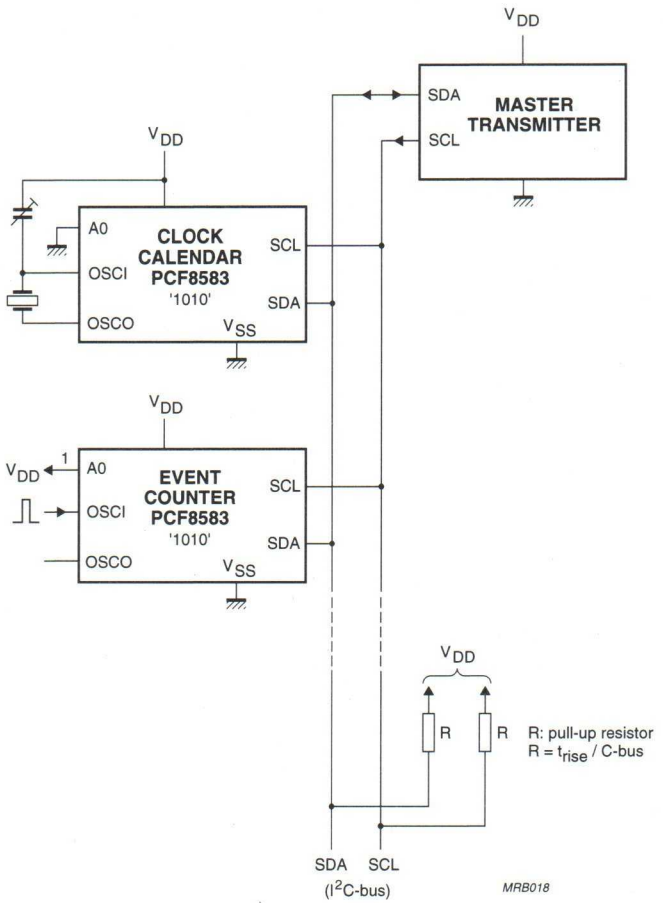


Fig.22 Application diagram.

Low power clock/calendar PCF8593

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Low power clock/calendar PCF8593

1 FEATURES

- I²C-bus interface operating supply voltage: 2.5 to 6.0 V
- Clock operating supply voltage (T_{amb} = 0 to +70 °C): 1.0 to 6.0 V
- 8 bytes scratchpad RAM (when alarm not used)
- Data retention voltage: 1.0 to 6.0 V
- External $\overline{\text{RESET}}$ input resets I²C interface (only)
- Operating current (f_{scl} = 0 Hz, 32 kHz time base, V_{DD} = 2.0 V): typ. 1 µA
- Clock function with four year calendar
- Universal timer with alarm and overflow indication
- 24 or 12 hour format
- 32.768 kHz or 50 Hz time base
- Serial input/output bus (I²C-bus)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function
- Space-saving SO8 package available
- Slave address:
  - READ A3
  - WRITE A2.

2 GENERAL DESCRIPTION

The PCF8593 is a CMOS clock/calendar circuit, optimized for low power consumption. Addresses and data are transferred serially via the two-line bidirectional I²C-bus. The built-in word address register is incremented automatically after each written or read data byte.
The built-in 32.768 kHz oscillator circuit and the first 8 bytes of RAM are used for the clock/calendar and counter functions. The next 8 bytes may be programmed as alarm registers or used as free RAM space.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage operating mode	I²C-bus active	2.5	–	6.0	V
		I²C-bus inactive	1.0	–	6.0	V
I_{DD}	supply current operating mode	f_{scl} = 100 kHz	–	–	200	µA
I_{DD}	supply current clock mode	f_{scl} = 0 Hz; V_{DD} = 5 V	–	4.0	15.0	µA
		f_{scl} = 0 Hz; V_{DD} = 2 V	–	1.0	8.0	µA
T_{amb}	operating ambient temperature		−40	–	+85	°C
T_{stg}	storage temperature		−65	–	+150	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8593P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCF8593T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

5 BLOCK DIAGRAM

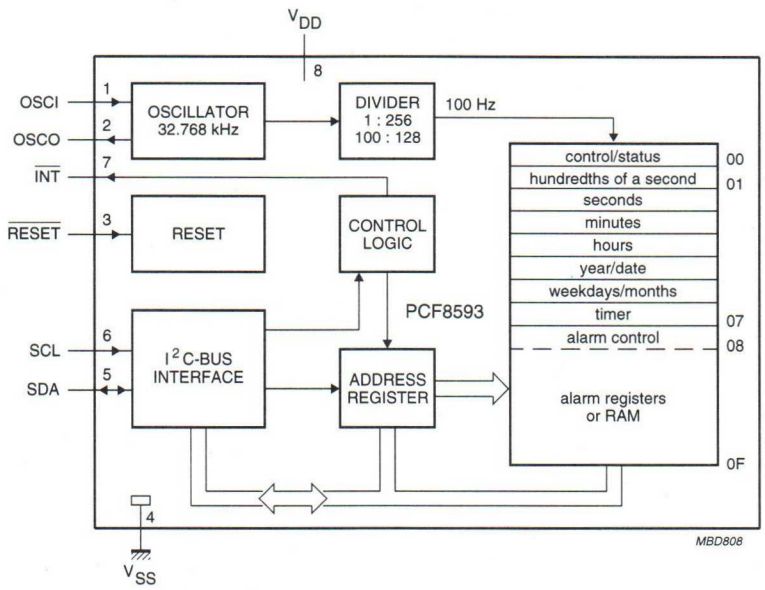


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
OSCI	1	oscillator input, 50 Hz or event-pulse input
OSCO	2	oscillator output
$\overline{\text{RESET}}$	3	reset input (active LOW)
V_{SS}	4	negative supply
SDA	5	serial data input/output
SCL	6	serial clock input
$\overline{\text{INT}}$	7	open drain interrupt output (active LOW)
V_{DD}	8	positive supply

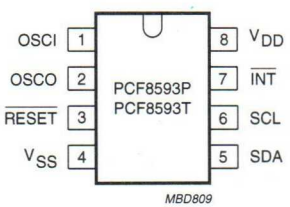


Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

The PCF8593 contains sixteen 8-bit registers with an 8-bit auto-incrementing address register, an on-chip 32.768 kHz oscillator circuit, a frequency divider and a serial two-line bidirectional I^2C-bus interface.

The first 8 registers (memory addresses 00 to 07) are designed as addressable 8-bit parallel registers. The first register (memory address 00) is used as a control/status register. The memory addresses 01 to 07 are used as counters for the clock function. The memory addresses 08 to 0F may be programmed as alarm registers or used as free RAM locations.

7.1 Counter function modes

When the control/status register is programmed, a 32.768 kHz clock mode, a 50 Hz clock mode or an event-counter mode can be selected.

In the clock modes the hundredths of a second, seconds, minutes, hours, date, month (four year calendar) and weekday are stored in a BCD format. The timer register stores up to 99 days. The event counter mode is used to count pulses applied to the oscillator input (OSCO left open-circuit). The event counter stores up to 6 digits of data.

When one of the counters is read (memory locations 01 to 07), the contents of all counters are strobed into capture latches at the beginning of a read cycle. Therefore, faulty reading of the count during a carry condition is prevented.

When a counter is written, other counters are not affected.

7.2 Alarm function modes

By setting the alarm enable bit of the control/status register the alarm control register (address 08) is activated.

By setting the alarm control register a dated alarm, a daily alarm, a weekday alarm or a timer alarm may be programmed. In the clock modes, the timer register (address 07) may be programmed to count hundredths of a second, seconds, minutes, hours or days. Days are counted when an alarm is not programmed.

Whenever an alarm event occurs the alarm flag of the control/status register is set. A timer alarm event will set the alarm flag and an overflow condition of the timer will set the timer flag. The open-drain interrupt output is switched on (active LOW) when the alarm or timer flag is set (enabled). The flags remain set until directly reset by a write operation.

When the alarm is disabled (Bit 2 of control/status register = 0) the alarm registers at addresses 08 to 0F may be used as free RAM.

7.3 Control/status register

The control/status register is defined as the memory location 00 with free access for reading and writing via the I^2C-bus. All functions and options are controlled by the contents of the control/status register (see Fig.3).

7.4 Counter registers

In the clock modes 24 h or 12 h format can be selected by setting the most significant bit of the hours counter register. The format of the hours counter is shown in Fig.5.

The year and date are packed into memory location 05 (see Fig 6). The weekdays and months are packed into memory location 06 (see Fig.7). When reading these memory locations the year and weekdays are masked out when the mask flag of the control/status register is set. This allows the user to read the date and month count directly.

In the event-counter mode events are stored in BCD format. D5 is the most significant and D0 the least significant digit. The divider is by-passed.

In the different modes the counter registers are programmed and arranged as shown in Fig.4. Counter cycles are listed in Table 1.

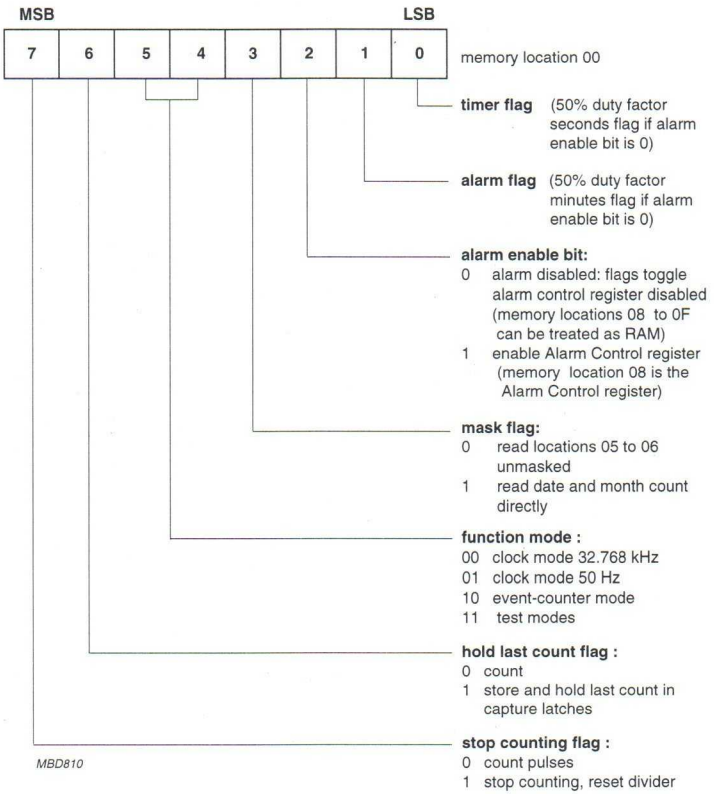


Fig.3 Control/status register.

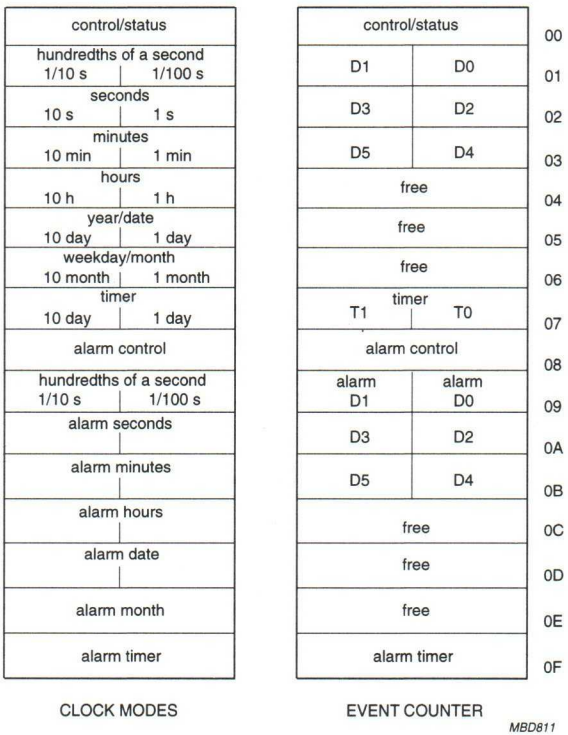


Fig.4 Register arrangement.

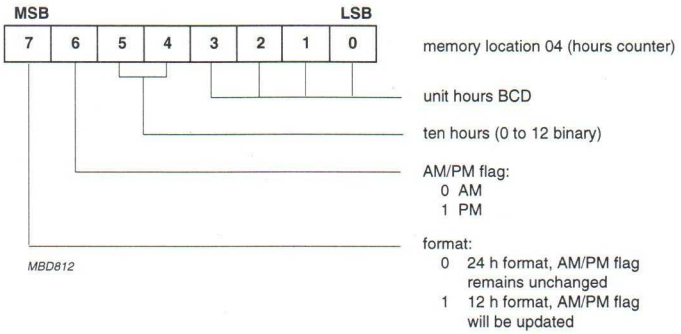


Fig.5 Format of the hours counter.

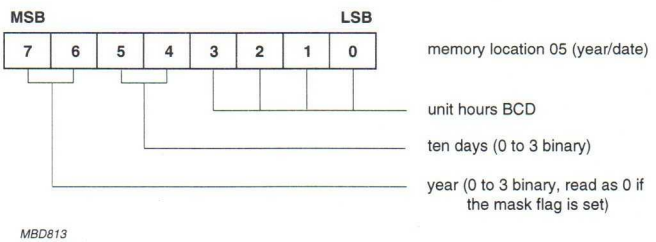


Fig.6 Format of the year/date counter.

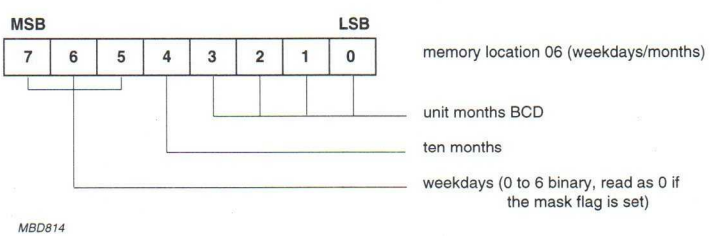


Fig.7 Format of the weekdays/months counter.

Table 1 Cycle length of the time counters, clock modes.

UNIT	COUNTING CYCLE	CARRY TO NEXT UNIT	CONTENTS OF THE MONTH COUNTER
Hundredths of a second	00 to 99	99 to 00	–
Seconds	00 to 59	59 to 00	–
Minutes	00 to 59	59 to 00	–
Hours (24 h)	00 to 23	23 to 00	–
Hours (12 h)	12 AM	–	–
	01 AM to 11 AM	–	–
	12 PM	–	–
	01 PM to 11 PM	11 PM to 12 AM	–
Date	01 to 31	31 to 01	1, 3, 5, 7, 8, 10 and 12
	01 to 30	30 to 01	4, 6, 9 and 11
	01 to 29	29 to 01	2, year = 0
	01 to 28	28 to 01	2, year = 1, 2 and 3
Months	01 to 12	12 to 01	–
Year	0 to 3	–	–
Weekdays	0 to 6	6 to 0	–
Timer	00 to 99	no carry	–

7.5 Alarm control register

When the alarm enable bit of the control/status register is set (address 00, bit 2) the alarm control register (address 08) is activated. All alarm, timer, and interrupt output functions are controlled by the contents of the alarm control register (see Fig.8).

7.6 Alarm registers

All alarm registers are allocated with a constant address offset of hexadecimal 08 to the corresponding counter registers (see Fig.4,Register arrangement).

An alarm signal is generated when the contents of the alarm registers matches bit-by-bit the contents of the involved counter registers. The year and weekday bits are ignored in a dated alarm. A daily alarm ignores the month and date bits. When a weekday alarm is selected, the contents of the alarm weekday/month register will select the weekdays on which an alarm is activated (see Fig.9).

Remark: in the 12 h mode, bits 6 and 7 of the alarm hours register must be the same as the hours counter.

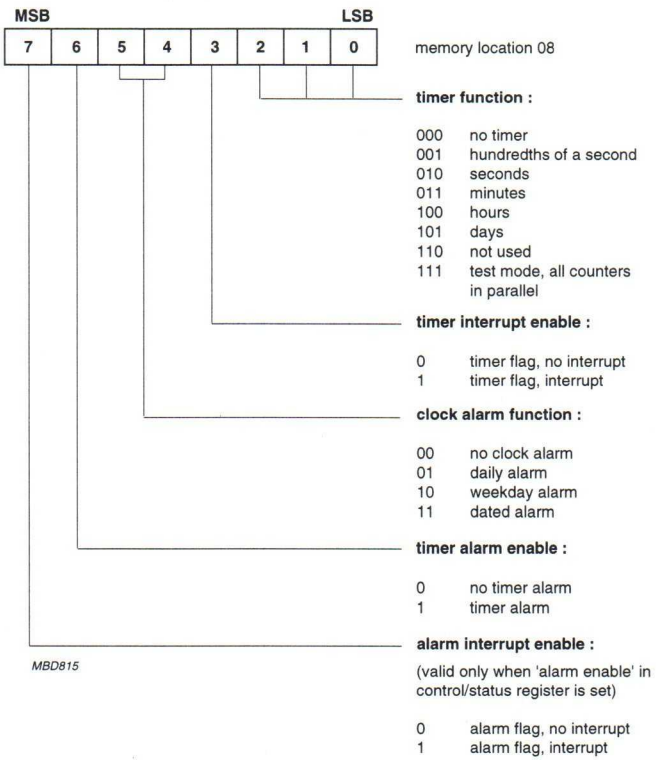


Fig.8 Alarm control register, clock mode.

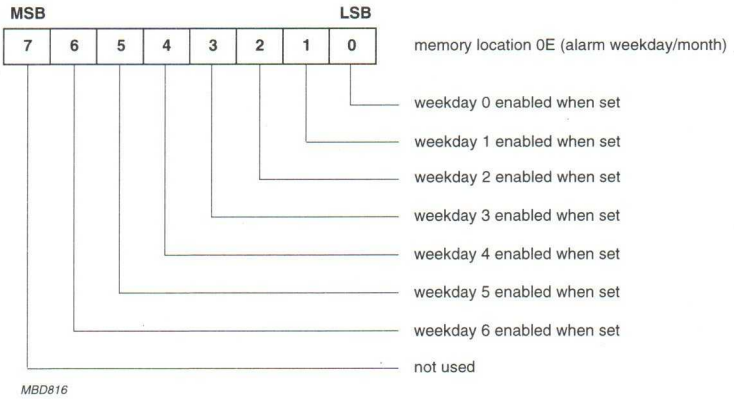


Fig.9 Selection of alarm weekdays.

7.7 Timer

The timer (location 07) is enabled by setting the control/status register = XX0X X1XX. The timer counts up from 0 (or a programmed value) to 99. On overflow, the timer resets to 0. The timer flag (LSB of control/status register) is set on overflow of the timer. This flag must be reset by software. The inverted value of this flag can be transferred to the external interrupt by setting bit 3 of the alarm control register.

Additionally, a timer alarm can be programmed by setting the timer alarm enable (bit 6 of the alarm control register). When the value of the timer equals a pre-programmed value in the alarm timer register (location 0F), the alarm flag is set (bit 1 of the control/status register). The inverted value of the alarm flag can be transferred to the external interrupt by enabling the alarm interrupt (bit 6 of the alarm control register).

Resolution of the timer is programmed via the 3 LSBs of the alarm control register (see Fig.11, Alarm and timer Interrupt logic diagram).

7.8 Event counter mode

Event counter mode is selected by bits 4 and 5 which are logic 1, 0 in the control/status register. The event counter mode is used to count pulses externally applied to the oscillator input (OSCO left open-circuit). The event counter stores up to 6 digits of data, which are stored as 6 hexadecimal values located in locations 1, 2, and 3. Thus, up to 1 million events may be recorded.

An event counter alarm occurs when the event counter registers match the value programmed in locations 9, A, and B, and the event alarm is enabled (bits 4 and 5 which are logic 0, 1 in the alarm control register). In this event, the alarm flag (bit 1 of the control/status register) is set. The inverted value of this flag can be transferred to the interrupt pin (pin 7) by setting the alarm interrupt enable in the alarm control register. In this mode, the timer (location 07) increments once for every one, one-hundred, ten thousand, or 1 million events, depending on the value programmed in bits 0,1 and 2 of the alarm control register. In all other events, the timer functions are as in the clock mode.

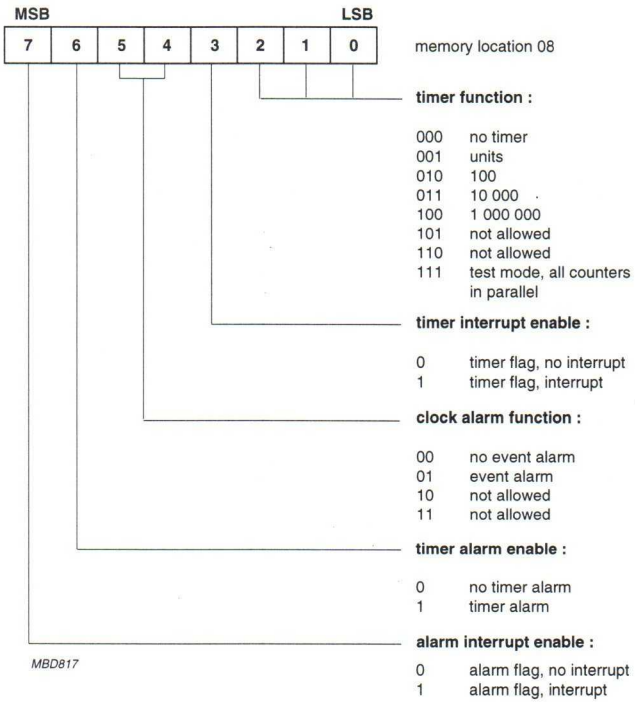
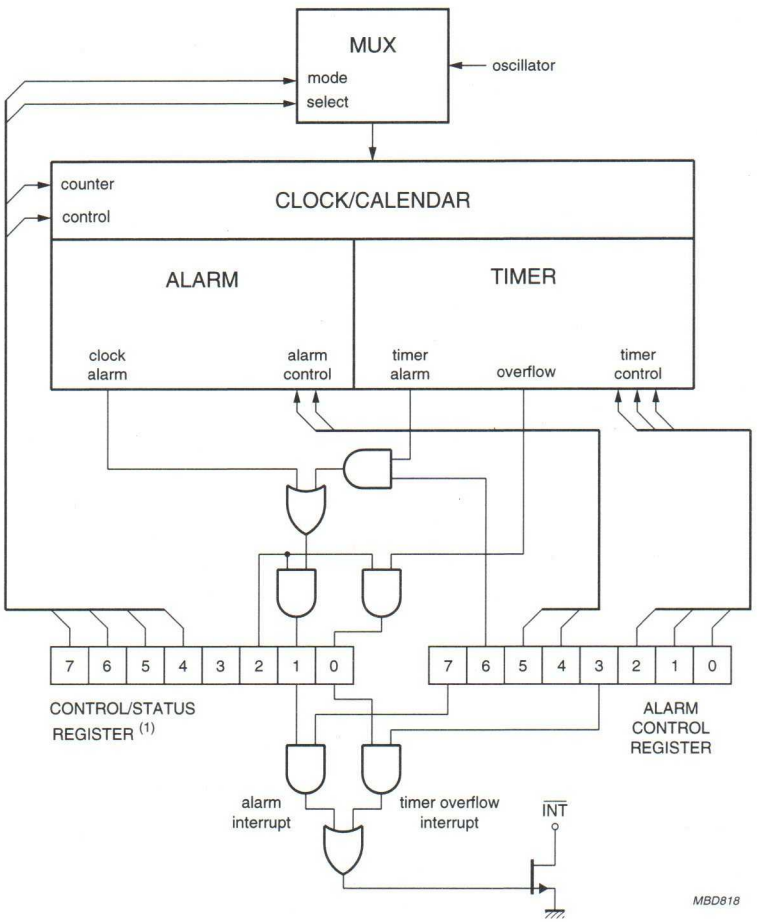


Fig.10 Alarm control register, event-counter mode.

7.9 Interrupt output

The conditions for activating the open-drain n-channel interrupt output $\overline{INT}$ (active LOW) are determined by appropriate programming of the alarm control register. These conditions are clock alarm, timer alarm, timer overflow, and event counter alarm. An interrupt occurs when the alarm flag or the timer flag is set, and the corresponding interrupt is enabled. In all events, the interrupt is cleared only by software resetting of the flag which initiated the interrupt.

In the clock mode, if the alarm enable is not activated (alarm enable bit of control/status register is logic 0), the interrupt output toggles at 1 Hz with a 50% duty cycle (may be used for calibration). The OFF voltage of the interrupt output may exceed the supply voltage, up to a maximum of 6.0 V. A logic diagram of the interrupt output is shown in Fig.11.



(1) If the alarm enable bit of the control/status register is reset (logic 0), a 1 Hz signal can be observed on the interrupt pin $\overline{INT}$.

Fig.11 Alarm and timer interrupt logic diagram.

7.10 Oscillator and divider

A 32.768 kHz quartz crystal has to be connected to OSCI (pin 1) and OSCO (pin 2). A trimmer capacitor between OSCI and V_{DD} is used for tuning the oscillator (see Chapter 14, Section 14.1). A 100 Hz clock signal is derived from the quartz oscillator for the clock counters.

In the 50 Hz clock mode or event-counter mode the oscillator is disabled and the oscillator input is switched to a high-impedance state. This allows the user to feed the 50 Hz reference frequency or an external high-speed event signal into the input OSCI.

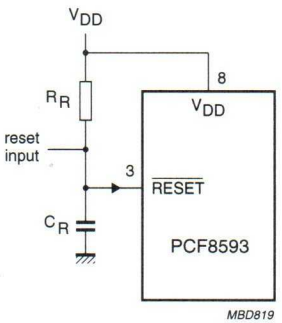
7.10.1 DESIGNING

When designing the printed-circuit board layout, keep the oscillator components as close to the IC package as possible, and keep all other signal lines as far away as possible. In applications involving tight packing of components, shielding of the oscillator may be necessary. AC coupling of extraneous signals can introduce oscillator inaccuracy.

7.11 Initialization (see Fig.12)

Note that immediately following power-on, all internal registers are undefined and, following a $\overline{\text{RESET}}$ pulse on pin 3, must be defined via software. Attention should be paid to the possibility that the device may be initially in event-counter mode, in which event the oscillator will not operate. Over-ride can be achieved via software.

Reset is accomplished by applying an external $\overline{\text{RESET}}$ pulse (active LOW) at pin 3. When reset occurs only the I^2C-bus interface is reset. The control/status register and all clock counters are not affected by $\overline{\text{RESET}}$. $\overline{\text{RESET}}$ must return HIGH during device operation.



To avoid overload of the internal diode by falling V_{DD}, an external diode should be added in parallel to R_R if $C_R \geq 0.2\ \mu F$. Note that RC must be evaluated with the actual V_{DD} of the application, as their value will be V_{DD} rise-time dependent.

Fig.12 RC reset.

An RC combination can also be utilized to provide a power-on $\overline{\text{RESET}}$ signal at pin 3. In this event, the values of the RC must fulfil the following relationship to guarantee power-on reset (see Fig.12).

$\overline{\text{RESET}}$ input must be $\leq 0.3V_{DD}$ when V_{DD} reaches V_{DDmin} (or higher).

It is recommended to set the stop counting flag of the control/status register before loading the actual time into the counters. Loading of illegal states may lead to a temporary clock malfunction.

8 CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

8.1 Bit transfer (see Fig.13)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

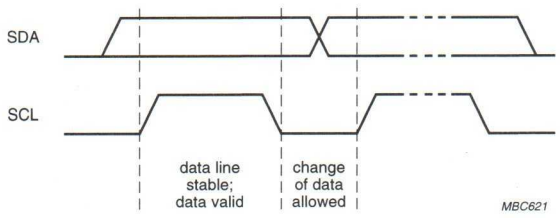


Fig.13 Bit transfer.

8.2 Start and stop conditions (see Fig.14)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

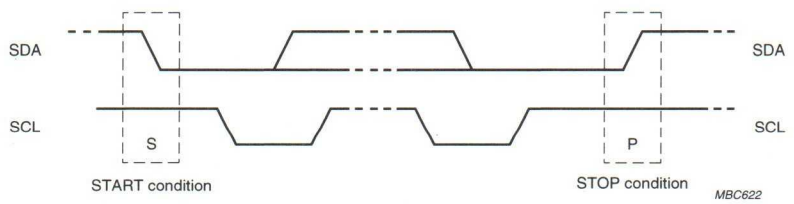


Fig.14 Definition of start and stop conditions.

8.3 System configuration (see Fig.15)

A device generating a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves'.

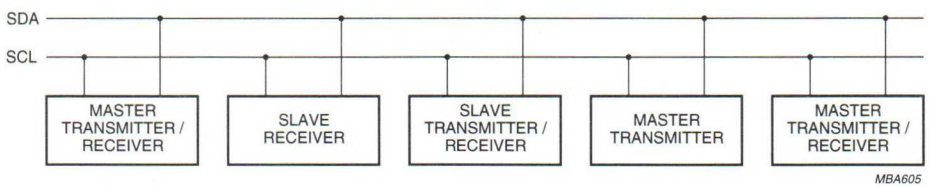


Fig.15 System configuration.

8.4 Acknowledge (see Fig.16)

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

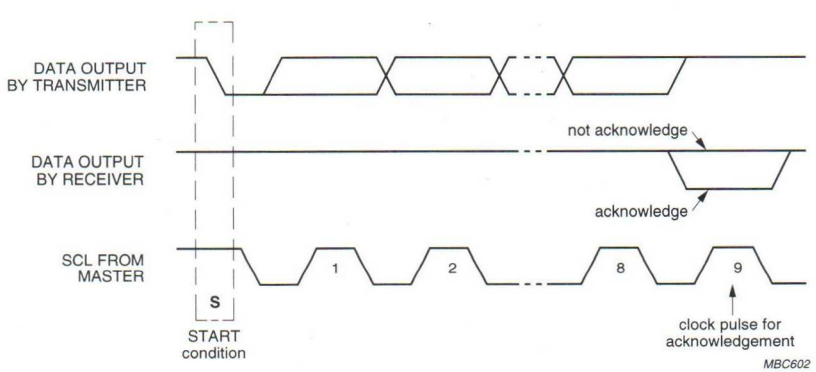


Fig.16 Acknowledgment on the I^2C-bus.

9 I²C-BUS PROTOCOL

9.1 Addressing

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure.

The clock/calendar acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line. The clock/calendar slave address is shown in Fig.17.

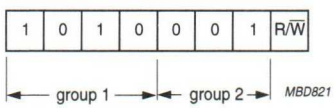


Fig.17 Slave address.

9.2 Clock/calendar READ/WRITE cycles

The I²C-bus configuration for the different PCF8593 READ and WRITE cycles is shown in Figs 18, 19 and 20.

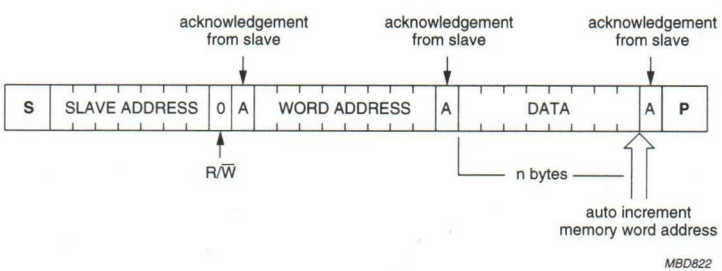


Fig.18 Master transmits to slave receiver (WRITE) mode.

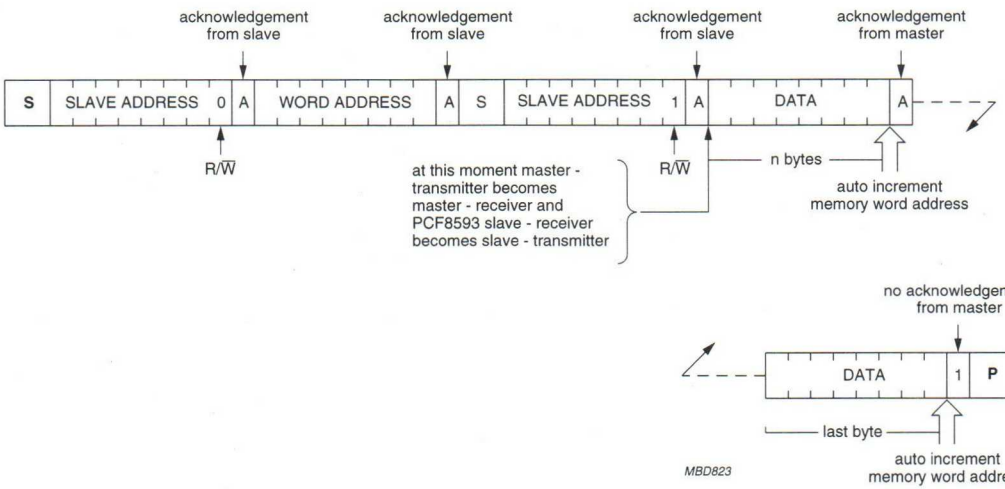


Fig.19 Master reads after setting word address (write word address, READ data).

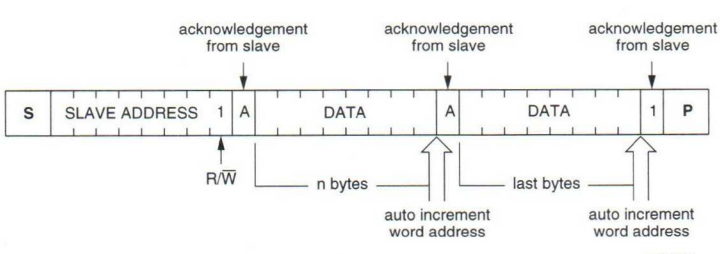


Fig.20 Master reads slave immediately after first byte (READ mode).

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (pin 8)	−0.8	+7.0	V
I_{DD}	supply current (pin 8)	−	50	mA
I_{SS}	supply current (pin 4)	−	50	mA
V_I	input voltage	−0.8	V_{DD} + 0.8	V
I_I	input current	−	10	mA
I_O	DC output current	−	10	mA
P_{tot}	total power dissipation per package	−	300	mW
P_O	power dissipation per output	−	50	mW
T_{amb}	operating ambient temperature	−40	+85	°C
T_{stg}	storage temperature	−65	+150	°C

11 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take precautions appropriate to handling MOS devices Advice can be found in Data Handbook IC12 under *"Handling MOS Devices"*.

12 DC CHARACTERISTICS

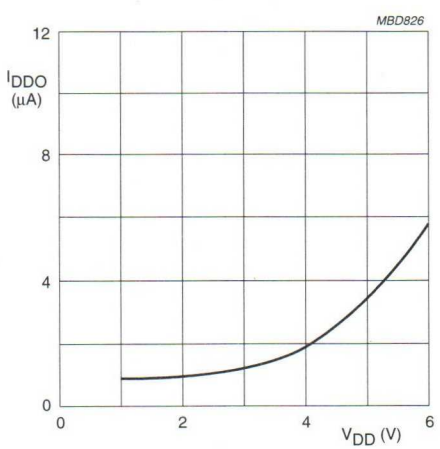
V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; f_{osc} = 32 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
Supply						
V_{DD}	supply voltage (operating mode)	I^2C-bus active	2.5	−	6.0	V
		I^2C-bus inactive	1.0	−	6.0	V
V_{DDosc}	supply voltage (quartz oscillator)	note 2				
		T_{amb} = 0 to 70 °C	1.0	−	6.0	V
		T_{amb} = −40 to 85 °C	1.2	−	6.0	V
I_{DD}	supply current (operating mode)	f_{scl} = 100 kHz; clock mode; note 3	−	−	200	µA
I_{DDO}	supply current (clock mode with I^2C-bus inactive)	f_{scl} = 0 Hz; inputs at V_{DD} or V_{SS}				
		V_{DD} = 2 V	−	1.0	8.0	µA
		V_{DD} = 5 V	−	4.0	15	µA
SDA, SCL, $\overline{INT}$ and RESET						
V_{IL}	LOW level input voltage		0	−	0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7V_{DD}	−	V_{DD}	V
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	−	−	mA
I_{LI}	input leakage current	V_I = V_{DD} or V_{SS}	−1	−	+1	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
C_i	input capacitance	note 4	–	–	7	pF
OSCI and $\overline{\text{RESET}}$						
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	−250	–	+250	nA
$\overline{\text{INT}}$						
I_{OL}	LOW level output current	V_{OL} = 0.4 V	1	–	–	mA
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	µA
SCL						
C_i	input capacitance	note 4	–	–	7	pF
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	−1	–	+1	µA

Notes

1. Typical values measured at T_{amb} = 25 °C.
2. When powering up the device, V_{DD} must exceed the specified minimum value by 300 mV to guarantee correct start-up of the oscillator.
3. Event counter mode: supply current dependent upon input frequency.
4. Tested on sample basis.



f_{SCL} = 32 kHz; T_{amb} = 25 °C.

Fig.21 Typical supply current in clock mode as a function of supply voltage.

13 AC CHARACTERISTICS

V_{DD} = 2.5 to 6.0 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator						
C_{osc}	integrated oscillator capacitance		20	25	30	pF
Δf_{osc}	oscillator stability	for ΔV_{DD} = 100 mV; T_{amb} = 25 °C; V_{DD} = 1.5 V	–	2×10^{-7}	–	
f_i	input frequency	note 1	–	–	1	MHz
Quartz crystal parameters (f = 32.768 kHz)						
R_s	series resistance		–	–	40	kΩ
C_L	parallel load capacitance		–	10	–	pF
C_T	trimmer capacitance		5	–	25	pF
I²C-bus timing (see Fig.22; notes 2 and 3)						
f_{SCL}	SCL clock frequency		–	–	100	kHz
t_{SP}	tolerable spike width on bus		–	–	100	ns
t_{BUF}	bus free time		4.7	–	–	µs
$t_{SU;STA}$	START condition set-up time		4.7	–	–	µs
$t_{HD;STA}$	START condition hold time		4.0	–	–	µs
t_{LOW}	SCL LOW time		4.7	–	–	µs
t_{HIGH}	SCL HIGH time		4.0	–	–	µs
t_r	SCL and SDA rise time		–	–	1.0	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{VD;DAT}$	SCL LOW to data out valid		–	–	3.4	µs
$t_{SU;STO}$	STOP condition set-up time		4.0	–	–	µs

Notes

1. Event counter mode only.
2. All timing values are valid within the operating supply voltage and ambient temperature range and reference to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.
3. A detailed description of the I²C-bus specification, with applications, is given in brochure *"The I²C-bus and how to use it"*. This brochure may be ordered using the code 9398 393 40011.

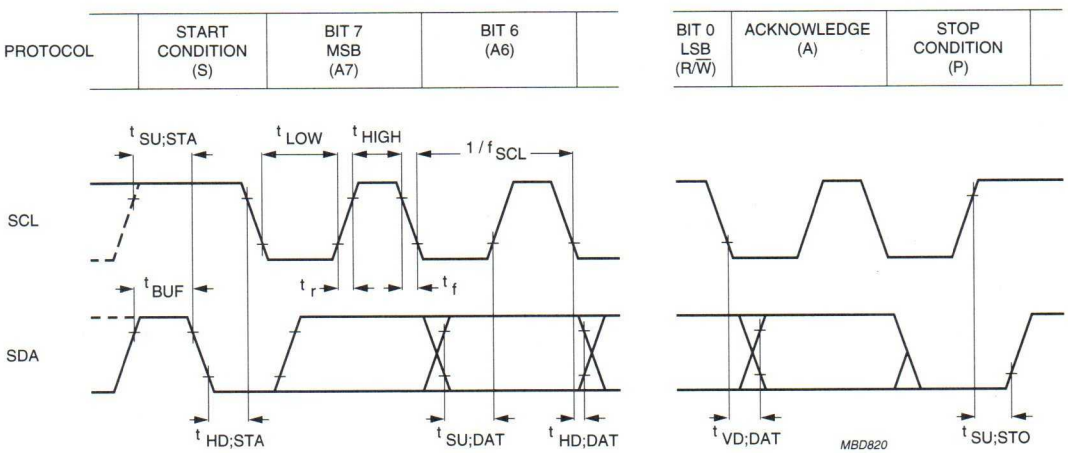


Fig.22 I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

14 APPLICATION INFORMATION

14.1 Quartz frequency adjustment

14.1.1 METHOD 1: FIXED OSCI CAPACITOR

By evaluating the average capacitance necessary for the application layout a fixed capacitor can be used. The frequency is best measured via the 1 Hz signal which can be programmed to occur at the interrupt output (pin 7). The frequency tolerance depends on the quartz crystal tolerance, the capacitor tolerance and the device-to-device tolerance (on average $\pm 5 \times 10^{-6}$). Average deviations of ±5 minutes per year can be achieved.

14.1.2 METHOD 2: OSCI TRIMMER

Using the alarm function (via the I²C-bus) a signal faster than 1 Hz can be generated at the interrupt output for fast setting of a trimmer.

Procedure:

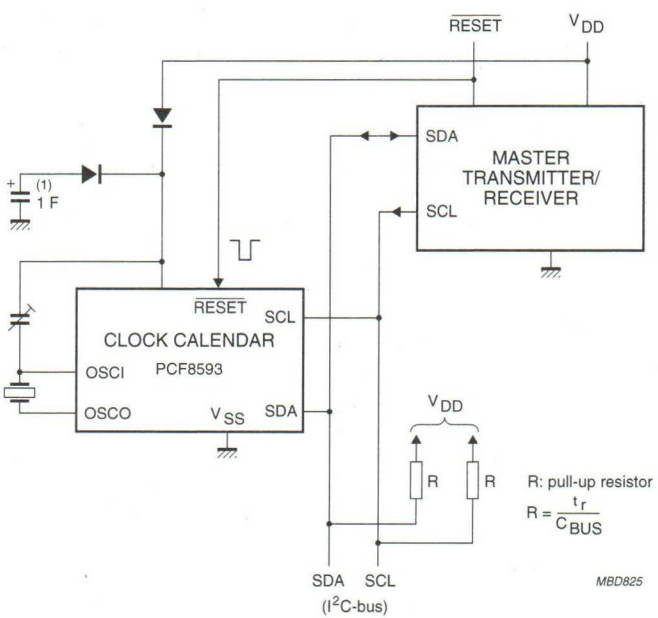
- Power-on
- Apply $\overline{\text{RESET}}$
- Initialization (alarm functions).

Routine:

- Set clock to time T and set alarm to time T + ΔT
- At time T + ΔT (interrupt) repeat routine.

14.1.3 METHOD 3: DIRECT OUTPUT

Direct measurement of oscillator output (accounting for test probe capacitance).



(1) Example Philips DLC 196 Double-Layer Capacitor family.

Fig.23 Application diagram.

PACKAGE INFORMATION

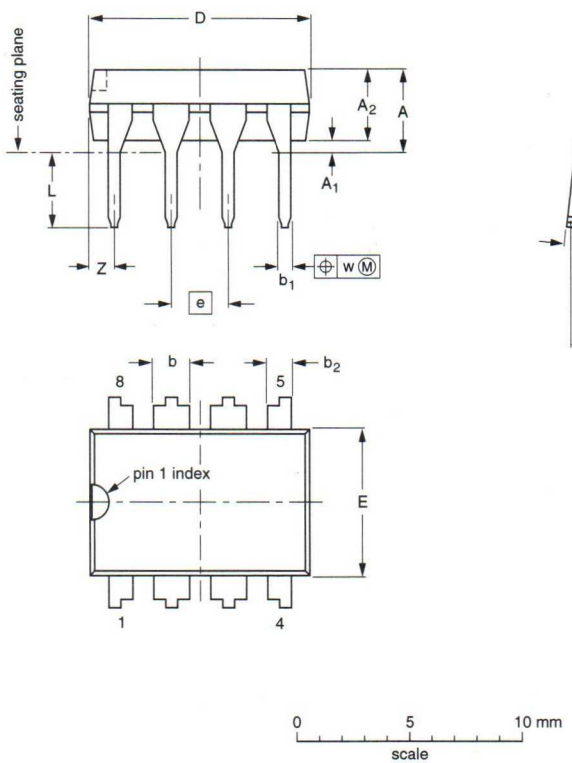
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DIP	219
PMFP	221
SO	222
VSO	226
Soldering	227

INDEX

NAME	DESCRIPTION	VERSION	PAGE
DIP (dual in-line package)			
DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1	
DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1	
PMFP8 (plastic micro flat package)			
PMFP8	plastic micro flat package; 8 leads (straight)	SOT144-1	
SO (small outline)			
SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1	
SO8	plastic small outline package; 8 leads (straight); body width 3.9 mm	SOT96-2	
SO8	plastic small outline package; 8 leads; body width 7.5 mm	SOT176-1	
SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1	
SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1	
VSO (very small outline)			
VSO40	plastic very small outline package; 40 leads; face down	SOT158-2	

DIP

DIP8: plastic dual in-line package; 8 leads (300 mil) SOT97-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

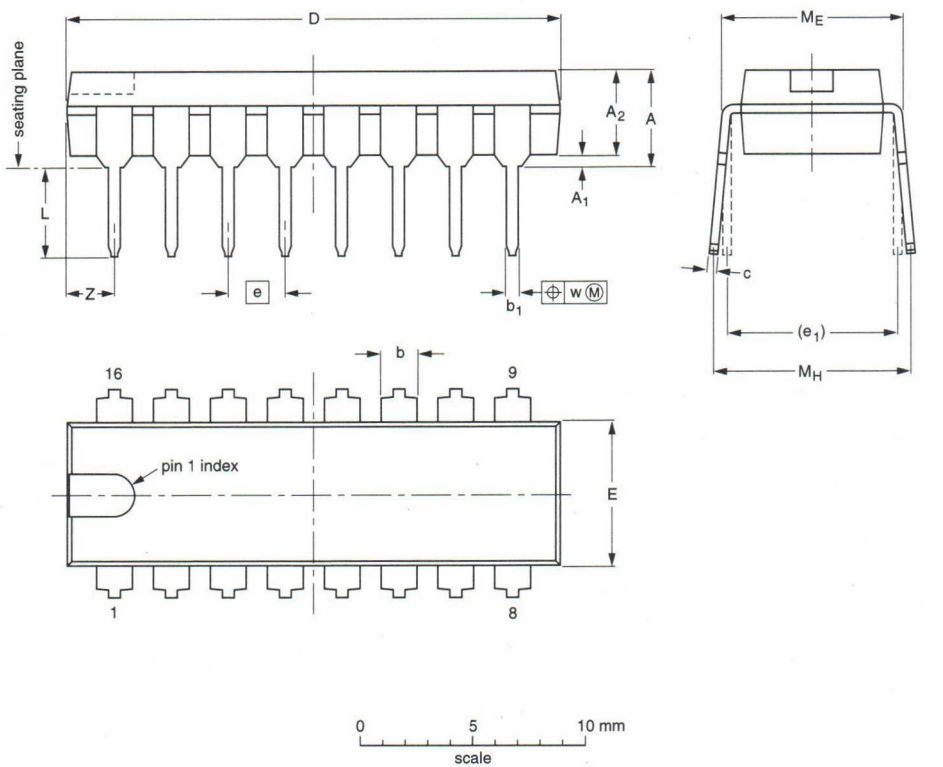
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D(1)	E(1)	e	e_1	L	M_E	M_H	w	Z(1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001AN				~~92-11-17~~ 95-02-04

DIP16: plastic dual in-line package; 16 leads (300 mil); long body SOT38-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

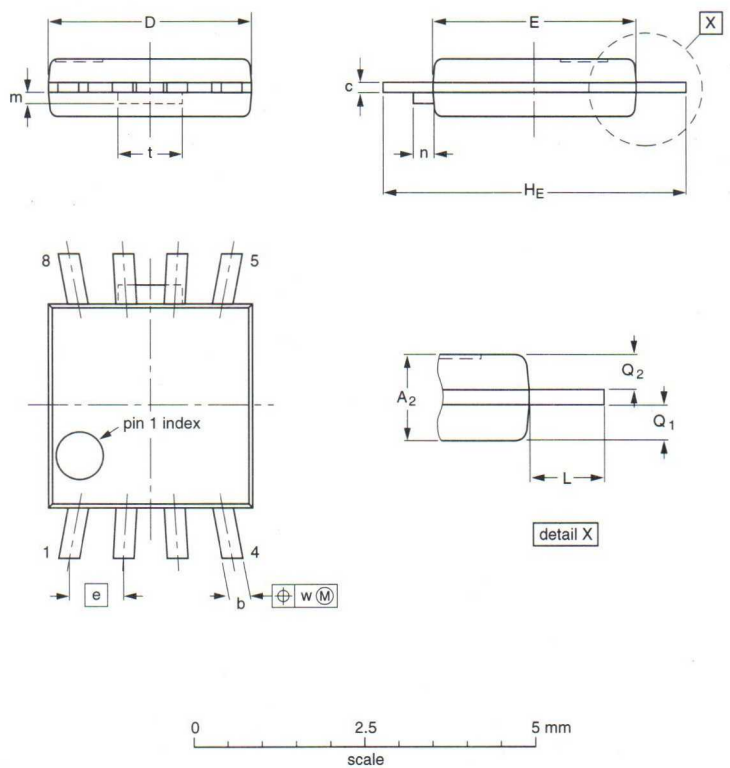
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				~~92-10-02~~ 95-01-19

PMFP

PMFP8: plastic micro flat package; 8 leads (straight) SOT144-1



DIMENSIONS (mm are the original dimensions)

UNIT	A_2	b	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	m max.	n max.	Q_1	Q_2	t	w
mm	0.90 0.70	0.40 0.25	0.19 0.12	3.1 2.9	3.1 2.9	0.80	4.6 4.4	0.75	0.26	0.3	0.40 0.30	0.40 0.30	0.95	0.1

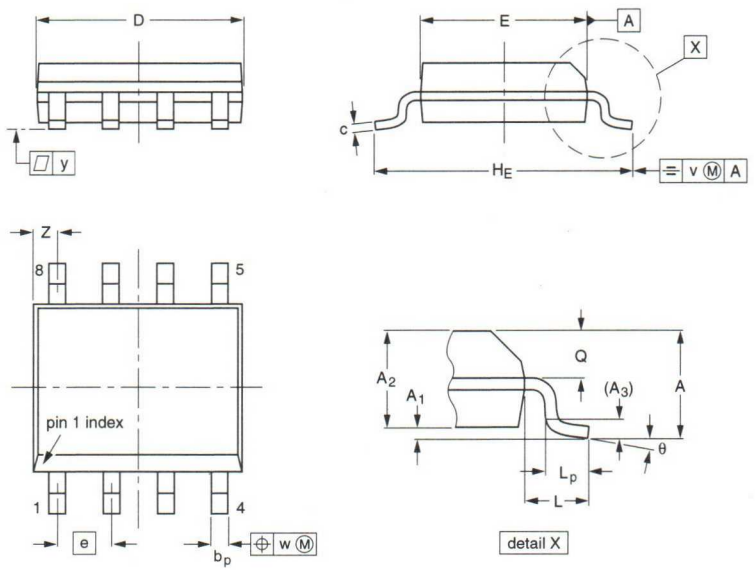
Note

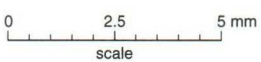
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT144-1						~~94-01-25~~ 95-01-24

SO

SO8: plastic small outline package; 8 leads; body width 3.9 mm SOT96-1





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

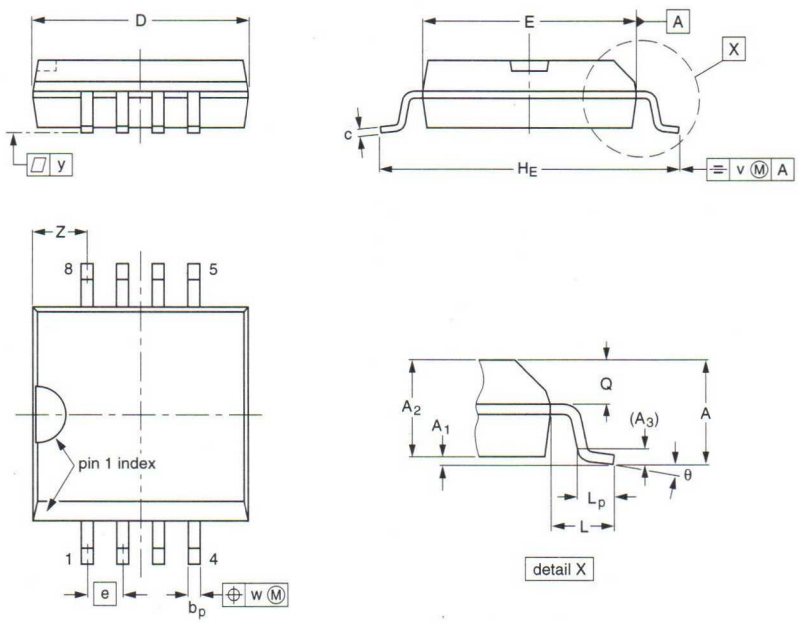
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~95-02-04~~ 97-05-22

SO8: plastic small outline package; 8 leads; body width 7.5 mm **SOT176-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

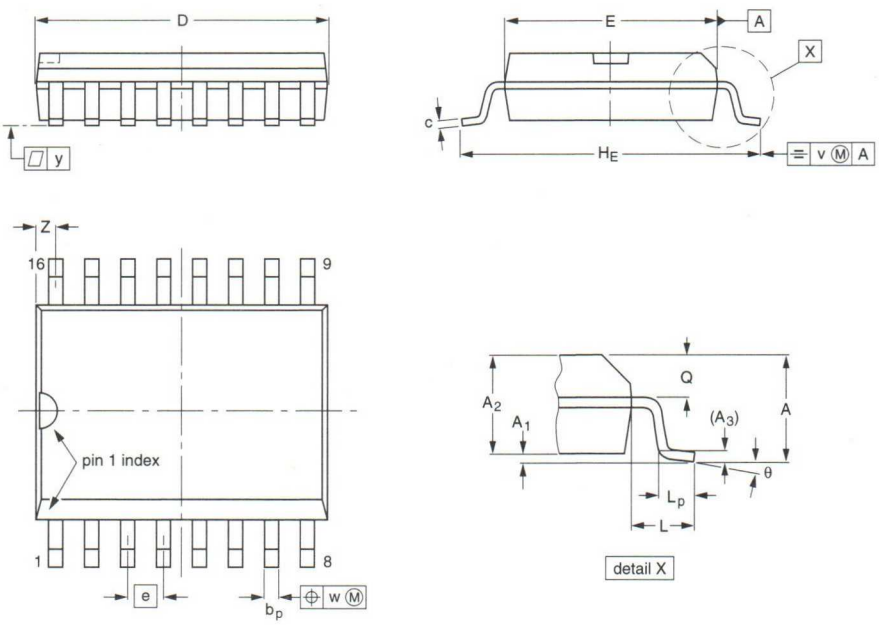
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	7.65 7.45	7.6 7.4	1.27	10.65 10.00	1.45	1.1 0.45	1.1 1.0	0.25	0.25	0.1	2.0 1.8	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.30 0.29	0.30 0.29	0.050	0.419 0.394	0.057	0.043 0.018	0.043 0.039	0.01	0.01	0.004	0.079 0.071	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT176-1						~~95-02-25~~ 97-05-22

SO16: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

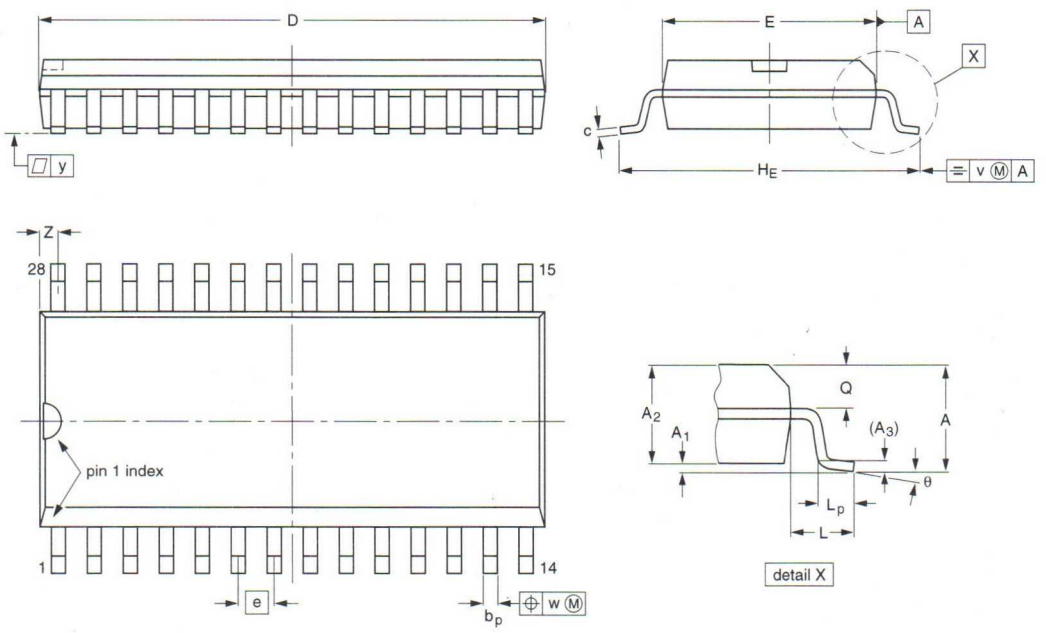
UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013AA				~~95-01-24~~ 97-05-22

SO28: plastic small outline package; 28 leads; body width 7.5 mm **SOT136-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

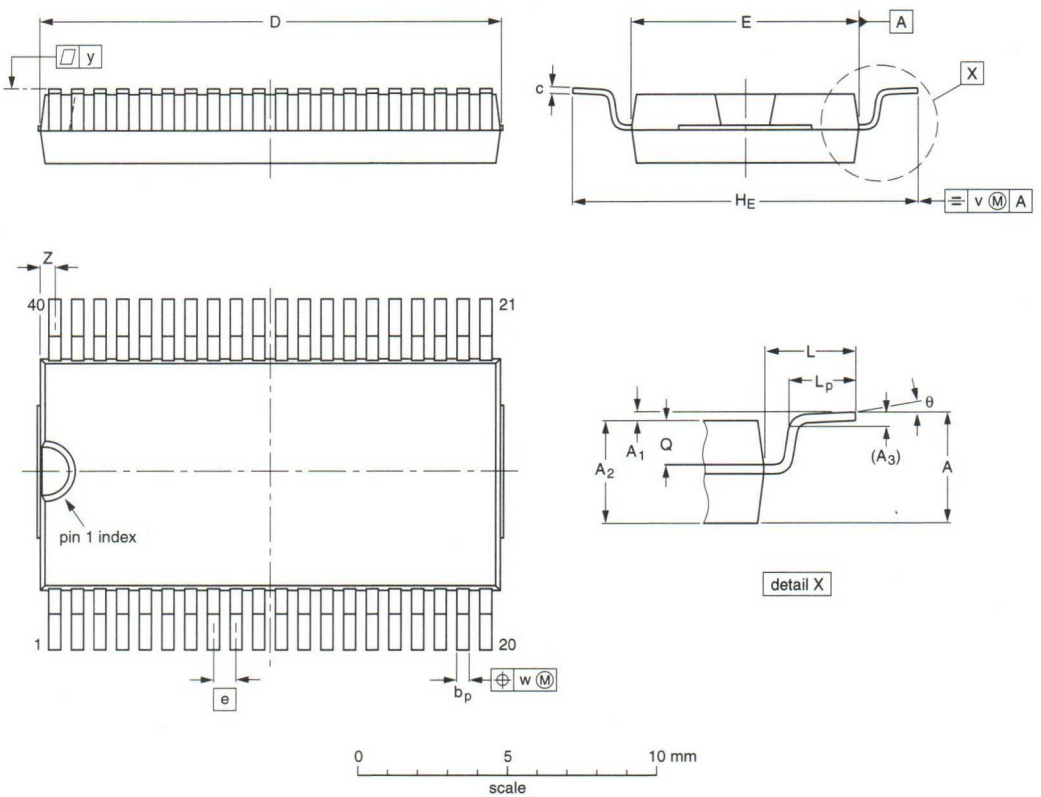
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~95-01-24~~ 97-05-22

VSO

VSO40: plastic very small outline package; 40 leads; face down SOT158-2



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.70	0.3 0.1	2.45 2.25	0.25	0.42 0.30	0.22 0.14	15.6 15.2	7.6 7.5	0.762	12.3 11.8	2.25	1.7 1.5	1.15 1.05	0.2	0.1	0.1	0.6 0.3	7° 0°
inches	0.11	0.012 0.004	0.096 0.089	0.010	0.017 0.012	0.0087 0.0055	0.61 0.60	0.30 0.29	0.03	0.48 0.46	0.089	0.067 0.059	0.045 0.041	0.008	0.004	0.004	0.024 0.012	

Note

1. Plastic or metal protrusions of 0.4 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT158-2						~~92-11-17~~ 95-01-24

INTRODUCTION

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9397 750 0011).

THROUGH-HOLE MOUNTED PACKAGES

Table 1 Types of through-hole mounted packages

TYPE	DESCRIPTION
DIP	plastic dual in-line package
SDIP	plastic shrink dual in-line package
HDIP	plastic heat-dissipating dual in-line package
DBS	plastic dual in-line bent from a single in-line package
SIL	plastic single in-line package

Soldering by dipping or wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SURFACE MOUNTED PACKAGES

Table 2 Types of surface mounted packages

TYPE	DESCRIPTION
SO	plastic small outline package
SSOP	plastic shrink small outline package
TSSOP	plastic thin shrink small outline package
VSO	plastic very small outline package
QFP	plastic quad flat package
LQFP	plastic low profile quad flat package
SQFP	plastic shrink quad flat package
TQFP	plastic thin quad flat package
PLCC	plastic leaded chip carrier

Reflow soldering

Reflow soldering techniques are suitable for all SMD packages, ease of soldering varies with the type of package as indicated in Table 3.

The choice of heating method may be influenced by larger plastic packages (QFP or PLCC with 44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information on moisture prevention, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Table 3 Suitability of surface mounted packages for various soldering methods: rating from 'a' to 'd': **'a' indicates most suitable** (soldering is not difficult); **'d' indicates least suitable** (soldering is achievable with difficulty).

PACKAGE TYPE	REFLOW METHOD					DOUBLE WAVE METHOD
	INFRARED	HOT BELT	HOT GAS	VAPOUR PHASE	RESISTANCE	
SO	a	a	a	a	d	a
SSOP	a	a	a	c	d	c
TSSOP	b	b	b	c	d	d
VSO	b	b	a	b	a	b
QFP	b	b	a	c	a	c
LQFP	b	b	a	c	d	d
SQFP	b	b	a	c	d	d
TQFP	b	b	a	c	d	d
PLCC	c	b	b	d	d	b

Wave soldering

Wave soldering is **not** recommended for SSOP, TSSOP, QFP, LQFP, SQFP or TQFP packages, this is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- For SSOP, TSSOP and VSO packages, the longitudinal axis of the package footprint must be parallel to the solder flow **and** must incorporate solder thieves at the downstream end.
- For QFP, LQFP and TQFP packages, the footprint must be at an angle of 45° to the board direction **and** must incorporate solder thieves downstream and at the side corners.

Even with these conditions, consider wave soldering only for the following package types:

- SO
- VSO
- PLCC
- SSOP **only with body width 4.4 mm**, e.g. SSOP16 (SOT369-1) or SSOP20 (SOT266-1).
- QFP **except** QFP52 (SOT379-1), QFP100 (SOT317-1, SOT317-2, SOT382-1) and QFP160 (SOT322-1); these are **not** suitable for wave soldering.
- LQFP **except** LQFP32 (SOT401-1), LQFP48 (SOT313-1, SOT313-2), LQFP64 (SOT314-2), LQFP80 (SOT315-1); these are **not** suitable for wave soldering.
- TQFP **except** TQFP64 (SOT357-1), TQFP80 (SOT375-1) and TQFP100 (SOT386-1); these are **not** suitable for wave soldering.

SQFP are **not** suitable for wave soldering.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Data handbook system

DATA HANDBOOK SYSTEM

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